LIN Transceiver with Voltage Regulator

Features

- Support Baud Rates up to 20 Kbaud with LIN-compatible output driver, 50 Kbaud with ISO9141 driver
- 43V load dump protected
- Wide supply voltage, 6.0V - 18.0V continuous:
  - Maximum input voltage of 30V
- Extended Temperature Range: -40 to +125°C
- Interface to PIC EUSART and standard USARTs
- Local Interconnect Network (LIN) bus pin:
  - Internal pull-up resistor and diode
  - Protected against ground shorts
  - Protected against loss of ground
  - High current drive
- Automatic thermal shutdown
- On-board Voltage Regulator:
  - Output voltage of 5.0V with tolerances of ±3% overtemperature range
  - Available with alternate output voltage of 3.3V with tolerances of ±3% overtemperature range
  - Maximum continuous input voltage of 30V
  - Internal thermal overload protection
  - Internal short circuit current limit
  - External components limited to filter capacitor only and load capacitor
- Two low-power modes:
  - Receiver on, Transmitter off, voltage regulator on (≅85 µA)
  - Receiver monitoring bus, Transmitter off, voltage regulator off (≅16 µA)

Description

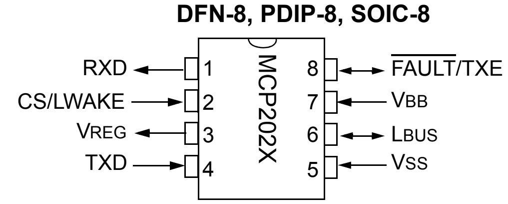
The MCP202X provides a bidirectional, half-duplex communication physical interface to automotive, and industrial LIN systems to meet the LIN bus specification Revision 2.0. The device incorporates a voltage regulator with 5V @ 50 mA or 3.3V @ 50 mA regulated power supply output. The regulator is short circuit protected, and is protected by an internal thermal shutdown circuit. The regulator has been specifically designed to operate in the automotive environment and will survive reverse battery connections, +43V load dump transients, and double-battery jumps. The device has been designed to meet the stringent quiescent current requirements of the automotive industry.

MCP202X family members:

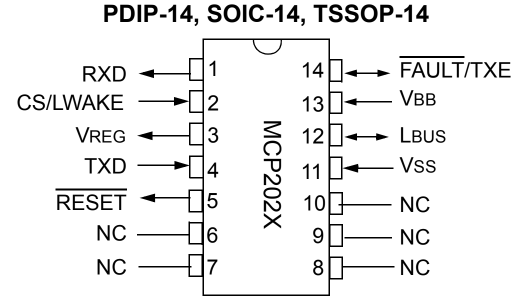
- 8-pin PDIP, DFN and SOIC packages:
  - MCP2021-330, LIN-compatible driver, 8-pin, 3.3V regulator
  - MCP2021-500, LIN-compatible driver, 8-pin, 5.0V regulator
- 14-lead PDIP, TSSOP and SOIC packages with $\overline{\text{RESET}}$ output:
  - MCP2022-330, LIN-compatible driver, 14-pin, 3.3V regulator
  - MCP2022-500, LIN-compatible driver, 14-pin, 5.0V regulator

Package Types

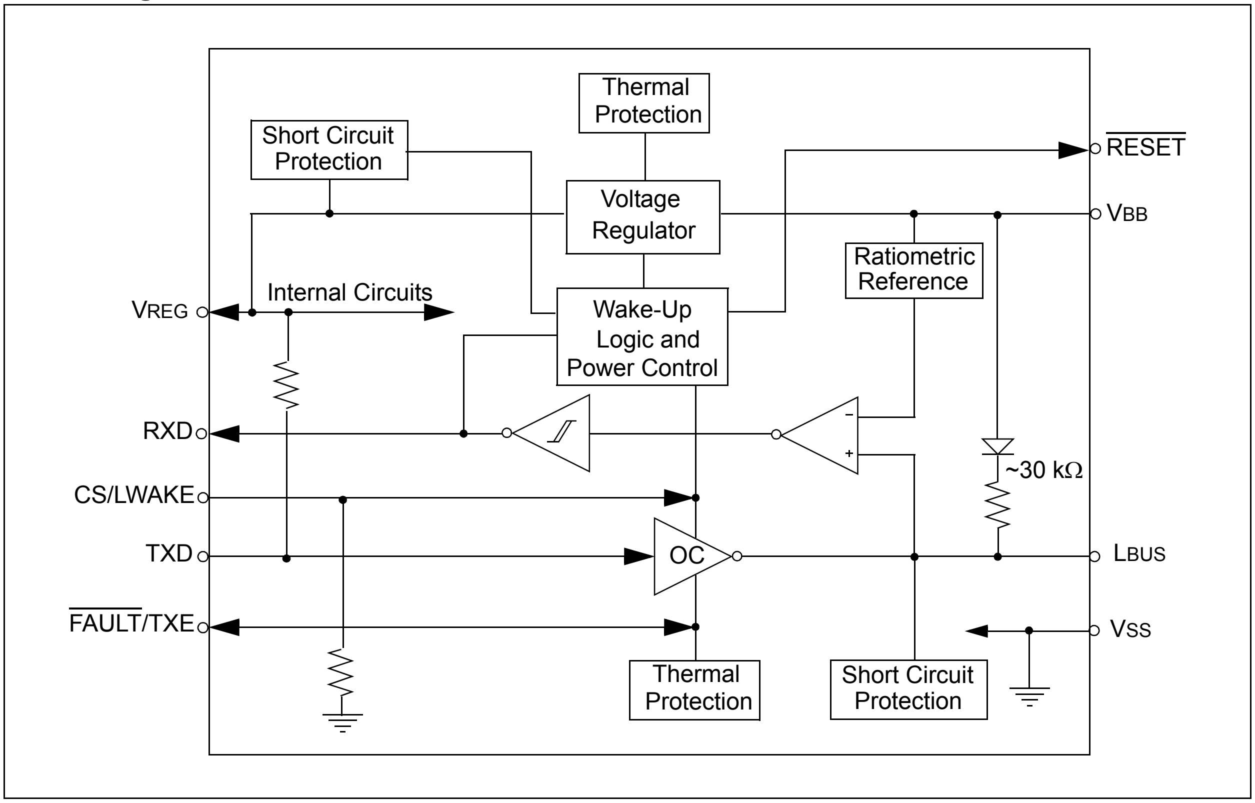
DFN-8, PDIP-8, SOIC-8



PDIP-14, SOIC-14, TSSOP-14



Block Diagram



 Preliminary

1.0 DEVICE OVERVIEW

The MCP202X provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus speeds up to 20 Kbaud.

The MCP202X provides a half-duplex, bidirectional communications interface between a microcontroller and the serial network bus. This device will translate the CMOS/TTL logic levels to LIN level logic, and vice versa.

The LIN specification 2.0 requires that the transceiver of all nodes in the system be connected via the LIN pin, referenced to ground and with a maximum external termination resistance of 510Ω from LIN bus to battery supply. The 510Ω corresponds to 1 Master and 16 Slave nodes.

The MCP2021-500 provides a +5V 50 mA regulated power output. The regulator uses a LDO design, is short-circuit-protected and will turn the regulator output off if it falls below 3.5V. The MCP202X also includes thermal shutdown protection. The regulator has been specifically designed to operate in the automotive environment and will survive reverse battery connections, +43V load dump transients and double-battery jumps. The other members of the MCP2021-330 family output +3.3V at 50 mA with a turn-off voltage of 2.5V. (see **Section 1.6 "Internal Voltage Regulator"**).

1.1 Optional External Protection

1.1.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see Figure 1-1).

1.1.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between V_{BB} and ground, with a 50Ω transient protection resistor (R_{TP}) in series with the battery supply and the V_{BB} pin serve to protect the device from power transients (see Example 1-1) and ESD events. While this protection is optional, it should be considered as good engineering practice.

EQUATION 1-1:

$$R_{TP} <= (V_{BB_{min}} - 5.5) / 250\ mA.$$
$$5.5V = V_{UVLO} + 1.0V,$$
250 mA is the peak current at power-on when $V_{BB} = 5.5V$

1.2 Internal Protection

1.2.1 ESD PROTECTION

For component-level ESD ratings, please refer to the maximum operation specifications.

1.2.2 GROUND LOSS PROTECTION

The LIN Bus specification states that the LIN pin must transition to the recessive state when ground is disconnected. Therefore, a loss of ground effectively forces the LIN line to a hi-impedance level.

1.2.3 THERMAL PROTECTION

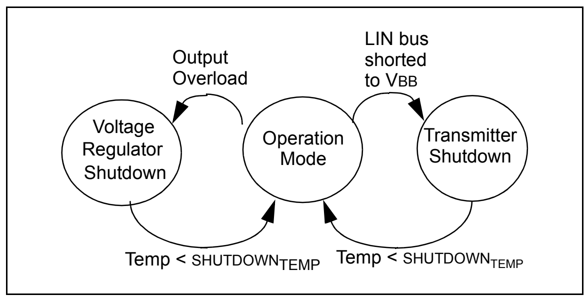
The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

There are three causes for a thermal overload. A thermal shut down can be triggered by any one, or a combination of, the following thermal overload conditions.

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (Rx = low, Tx = high) or a thermal overload condition (Rx = high, Tx = low).

FIGURE 1-1: THERMAL SHUTDOWN STATE DIAGRAMS



1.3 Modes of Operation

For an overview of all operational modes, please refer to Table 1-1.

1.3.1 POWER-ON-RESET MODE

Upon application of VBB, the device enters Power-On-Reset mode (POR). During this mode, the part maintains the digital section in a reset mode and waits until the voltage on pin VBB rises above the “ON” threshold (Typ. 5.75V) to enter to the Ready mode. If during the operation, the voltage on pin VBB falls below the “OFF” threshold (Typ. 4.25V), the part comes back to the Power-On-Reset mode.

1.3.2 POWER-DOWN MODE

In the Power-down mode, the transmitter and the voltage regulator are both off. Only the receiver section, and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g. a BREAK character) or CS/LWAKE going to a high level should occur during Power-down mode, the device will immediately enter the Ready mode, enable the voltage regulator, and once the output has stabilized (approximately 0.3 ms to 1.2 ms), go to the Operation mode.

Note:	The above time interval < 1.2 ms assumes 12V VBB input and no thermal shutdown event.

The part will also enter the Ready mode, followed by the Operation mode, if the CS/LWAKE pin should become active true (‘1’).

The part may only enter the Power-down mode after going through an Operation mode step.

1.3.3 READY MODE

Upon entering the Ready mode, the voltage regulator and receiver threshold detect circuit are powered up. The transmitter remains in power down mode. The device is ready to receive data but not to transmit. If a microcontroller is being driven by the voltage regulator output, it will go through a Power-on Reset and initialization sequence. The LIN pin is in the recessive state.

The device will stay in the Ready mode until the output of the voltage regulator has stabilized and CS/LWAKE pin is true (‘1’). After VREG is OK and CS/LWAKE pin is true, the transmitter is enabled and the part enters the Operation mode.

On Power-on of the VBB supply pin, the component will stay in the Ready mode if CS/LWAKE is low. If CS/LWAKE is high, the device will immediately enter the Operation mode.

1.3.4 OPERATION MODE

In this mode, all internal modules are operational.

The MCP202X will go into the Power-down mode on the falling edge of CS/LWAKE.

1.3.5 TRANSMITTER OFF MODE

Whenever the $\overline{\text{FAULT}}$/TXE signal is low and the LBUS transmitter is off.

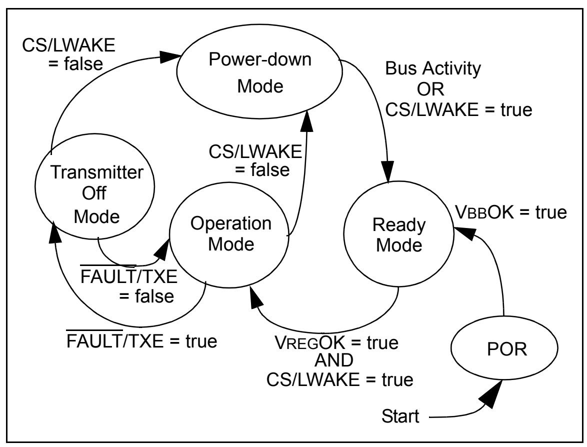
The transmitter may be re-enabled whenever the $\overline{\text{FAULT}}$/TXE signal returns high, either by removing the internal fault condition or the CPU returning the $\overline{\text{FAULT}}$/TXE high. The transmitter will not be enabled if the nFAULT/TXE pin is brought high when the internal fault is still present.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption of the bus during times of uncertain operation.

1.3.5.1 Wake-up

The Wake-up sub module observes the LBUS in order to detect bus activity. Bus activity is detected when the voltage on the LBUS stays below a threshold of approximately 3V for at least a typical duration of 10 µs. Such a condition causes the device to leave the Power-down mode.

FIGURE 1-2: OPERATIONAL MODES STATE DIAGRAMS



Note:	While the MCP202X is in shutdown, TXD should not be actively driven high or it may power internal logic through the ESD diodes and may damage the device.

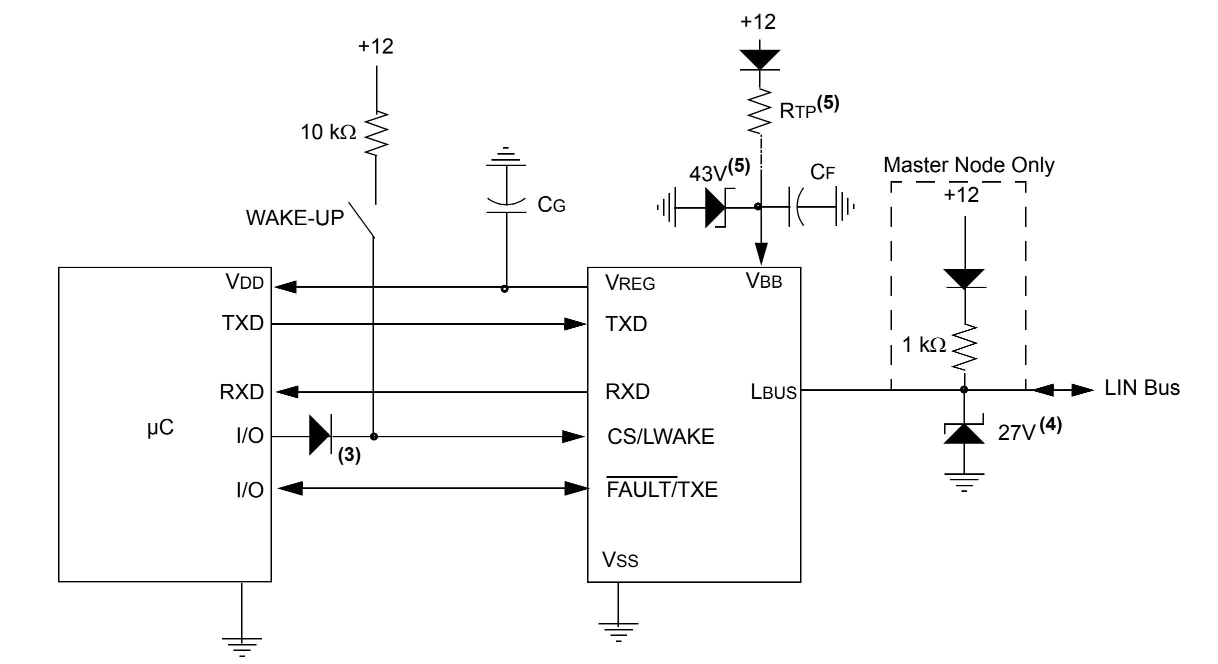
 Preliminary

TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Voltage Regulator	Operation	Comments
POR	OFF	OFF	OFF	Read CS/LWAKE, if LOW then READY, if HIGH Operational mode	
READY	OFF	Activity Detect	ON	If CS/LWAKE high level, then Operation mode	Bus Off state
OPERATION	ON	ON	ON	If CS/LWAKE low level, then Power down If FAULT/TXE low level, then Transmitter-Off mode	Normal Operation mode
POWERDOWN	OFF	Activity Detect	OFF	On LIN bus falling, go to READY mode. On CS/LWAKE high level, go to Operational mode	Low Power mode
TRANSMITTER-OFF	OFF	ON	ON	If CS/LWAKE low level, then Power down If FAULT/TXE high, then Operation mode	

1.4 Typical Applications

EXAMPLE 1-1: TYPICAL MCP2021 APPLICATION



Note 1: C_G is the load capacitor should be ceramic or tantalum rated for extended temperatures, 1.0-22 µF with ESR 0.4Ω - 5Ω.

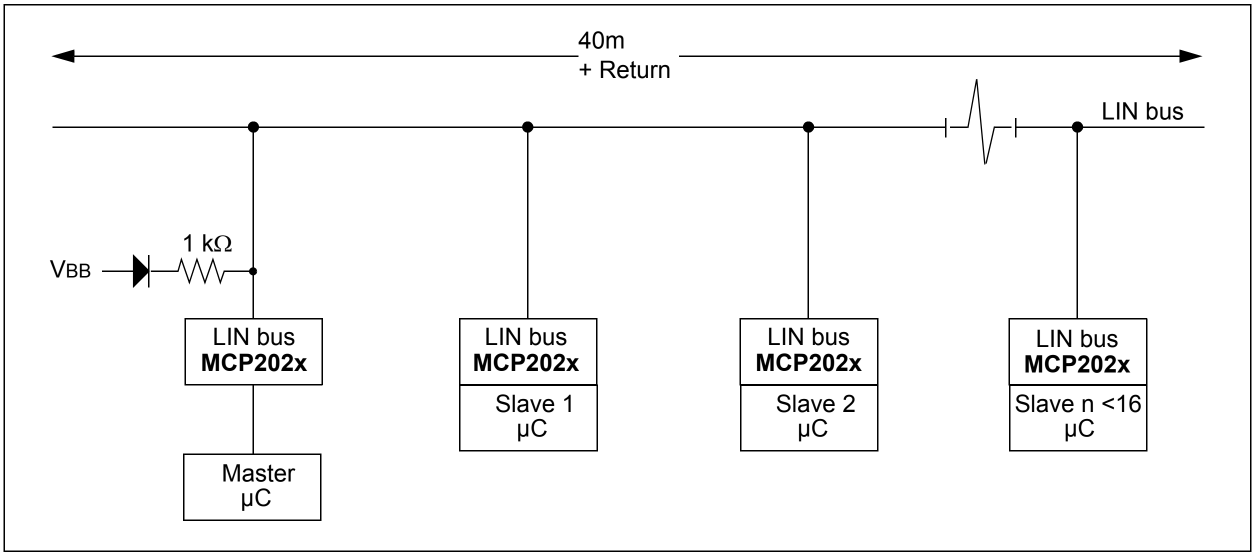
2: C_F is the filter capacitor for the external voltage supply.

3: This diode is only needed if CS/LWAKE is connected to 12V supply.

4: Transient suppressor diode. Vclamp L = 43V.

5: These components are for additional load dump protection.

FIGURE 1-3: TYPICAL LIN NETWORK CONFIGURATION



1.5 Pin Descriptions

TABLE 1-1: PINOUT DESCRIPTIONS

Pin Name	Devices: 8-Pin DFN, PDIP, SOIC	Devices: 14-Pin PDIP, SOIC, TSSOP	Pin Type	Function: Normal Operation
VREG	3	3	O	Power Output
VSS	5	11	P	Ground
VBB	7	13	P	Battery Supply
TXD	4	4	I	Transmit Data Input (TTL)
RXD	1	1	O	Receive Data Output (CMOS)
LBUS	6	12	I/O	LIN bus (bidirectional)
CS/LWAKE	2	2	TTL	Chip Select (TTL)
$\overline{\text{FAULT}}$/TXE	8	14	OD	Fault Detect Output, Transmitter Enable (OD)
$\overline{\text{RESET}}$	—	5	OD	$\overline{\text{RESET}}$ signal Output (OD)

Legend: TTL = TTL input buffer, ST = Schmitt Trigger input buffer, OD = Open-Drain output,
P = Power, O = Output, I = Input

1.5.1 POWER OUTPUT (VREG)

Positive Supply Voltage Regulator Output pin.

1.5.2 GROUND (VSS)

Ground pin.

1.5.3 BATTERY (VBB)

Battery Positive Supply Voltage pin. This pin is also the input for the internal voltage regulator.

1.5.4 TRANSMIT DATA INPUT (TXD)

The Transmit Data Input pin has an internal pull-up to VREG. The LIN pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

For extra bus security, TXD is internally forced to '1' when VREG is less than 1.8V (typ.).

In case the thermal protection detects an over-temperature condition while the signal TXD is low, the transmitter is shutdown. The recovery from the thermal shutdown is equal to adequate cooling time.

1.5.5 RECEIVE DATA OUTPUT (RXD)

The Receive Data Output pin is a standard CMOS output and follows the state of the LIN pin.

1.5.6 LIN BUS

The bidirectional LIN bus Interface pin is the driver unit for the LIN pin and is controlled by the signal TXD. LIN has an open collector output with a current limitation. To reduce EMI, the edges during the signal changes are slope-controlled. To further reduce radiated emissions, the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN Receiver observes the activities on LIN bus, and generates the output signal RXD that follows the state of the LBUS. A 1st degree 1 MHz, low-pass input filter is placed to maintain EMI immunity.

1.5.7 CS/LWAKE

Chip Select Input pin. A internal pull-down resistor will keep the CS/LWAKE pin low. This is done to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and I/O initialization sequence. The pin must see a high level to activate the transmitter.

If CS/LWAKE= '0' when the VBB supply is turned on, the device stays in Ready mode (Low-power mode). In Ready mode, both the receiver and the voltage regulator are on and the LIN transmitter driver is off.

If CS/LWAKE = '1' when the VBB supply is turned on, the device will proceed to the Operation mode as soon as the VREG output has stabilised.

This pin may also be used as a local wake-up input.(See Figure 1-2). In this implementation, the microcontroller will set the I/O pin that controls the CS/LWAKE as an high-impedance input. The internal pull-down resistor will keep the input low. An external switch, or other source, can then wake-up both the transceiver and the microcontroller.

1.5.8 FAULT/TXE

Fault Detect output and Transmitter Enable input bidirectional pin.

This pin is an open-drain output. Its state is defined as shown in Table 1-2. The transmitter driver is disabled whenever this pin is low (‘0’), either from an internal fault condition or by external drive. This allows the transmitter to be placed in an off state and still allow the voltage regulator to operate. Refer to Figure 1-4.

The FAULT/TXE also signals a mismatch between the TXD input and the LBUS level. This can be used to detect a bus contention. Since the bus exhibits a propagation delay, the sampling of the internal compare is debounced to eliminate false faults.

This pin has an internal pull-up resistor of approximately 750 kΩ.

> **Note 1:** The FAULT/TXE pin is true (0) whenever the internal circuits have detected a short or thermal excursion and have disabled the LBUS output driver.
>
> **2:** FAULT/TXE is true (0) when VREG not OK and has disabled the LBUS output driver.

The FAULT/TXE pin sampled at a rate faster than every 10 µs.

TABLE 1-2: FAULT/TXE TRUTH TABLE

TXD In	RXD Out	LINBUS I/O	Thermal Override	FAULT/TXE		Definition
				External Input	Driven Output	
L	H	VBB	OFF	H	L	**FAULT**, TXD driven low, LINBUS shorted to VBB **(Note 1)**
H	H	VBB	OFF	H	H	**OK**
L	L	GND	OFF	H	H	**OK**
H	L	GND	OFF	H	H	**OK**, data is being received from the LINBUS
x	x	VBB	ON	H	L	**FAULT**, Tranceiver in thermal shutdown
x	x	VBB	x	L	x	**NO FAULT**, the CPU is commanding the tranceiver to turn off the transmitter driver

Legend: x = don’t care

Note 1: The FAULT/TXE is valid after approximately 25 µs after TXD falling edge. This is to eliminate false fault reporting during bus propagation delays.

1.5.9 RESET

RESET is an open-drain output pin. This pin tracks an internal signal and indicates that the system voltage has reached the proper level and stabilized. It also operates as protection from brown-out conditions when the supply voltage drops below a safe operating voltage. The RESET is asserted immediately upon entering the Powerdown mode.

 Preliminary

1.6 Internal Voltage Regulator

1.6.1 5.0V REGULATOR

The MCP2021 has a low-drop-out voltage, positive regulator capable of supplying 5.00 VDC ±3% at up to 50 mA of load current over the entire operating temperature range of -40°C to +125°C. With a load current of 50 mA, the minimum input to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 µA with a full 50 mA load current when the input to output voltage differential is greater than +3.00V.

The regulator requires an external output bypass capacitor for stability. The capacitor should be either ceramic or tantalum for stable operation over the extended temperature range. The compensation capacitor should range from 1.0 µf – 22 µf and have a ESR or CSR of 10 MW – 3.0W. Aluminum, film, organic capacitors may also be used as long as they meet the capacitance and ESR requirements. Ceramic capacitors can have ESR values down below 10 MW.

Designed for automotive applications, the regulator will protect itself from double-battery jumps and up to +43V load dump transients. The voltage regulator has both short-circuit and thermal shutdown protection built-in.

Regarding the correlation between VBB, VREG and IDD, please refer to Figure 1-5 through 1-7. When the input voltage (VBB) drops below the differential needed to provide stable regulation, the output Vreg will track the input down to approximately 3.5V, at which point the regulator will turn off. This will allow microcontrollers with internal POR circuits to generate a clean arming of the Power-on Reset trip point. The MCP2021 will then monitor VBB and turn on the regulator when Vbb is 6.0V.

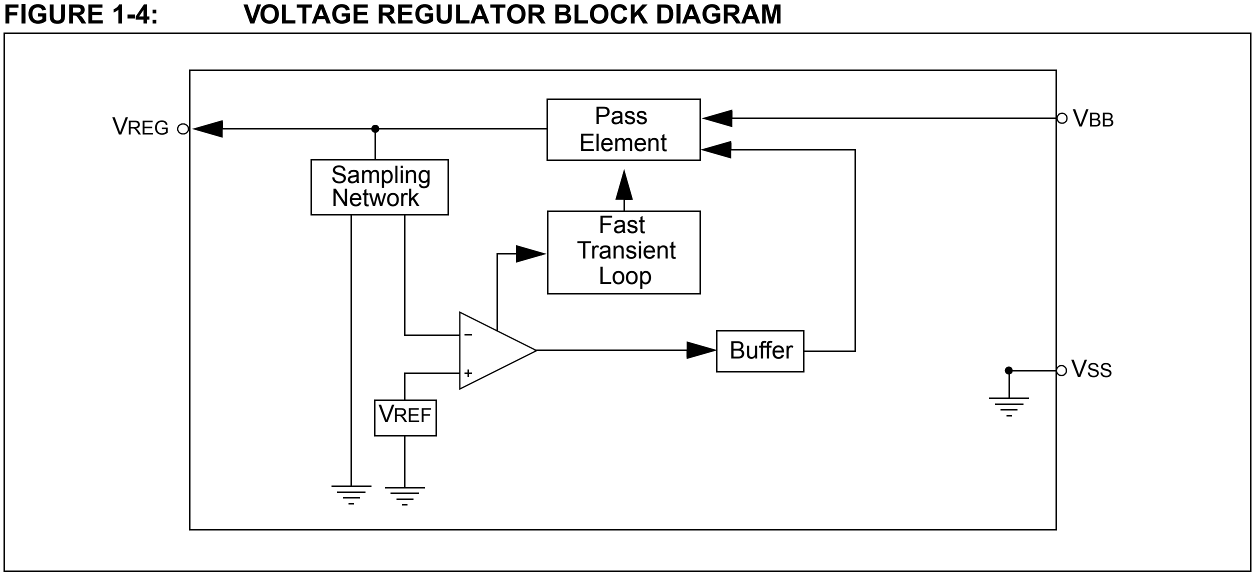
When the input voltage (VBB) drops below the differential needed to provide stable regulation, the output VREG) will track the input down to approximately +4.25V. The regulator will turn off the output at this point. This will allow PIC® microcontrollers, with internal POR circuits, to generate a clean arming of the Power-on Reset trip point. The regulator output will stay off until VBB is above +5.75 V_{DC}.

In the start phase, the device must see at least 6.0V to initiate operation during power up. In the Power-down mode, the VBB monitor will be turned off.

Note:	The regulator has an overload current limiting of approximately 100 mA. During a short circuit, the VREG is monitored. If VREG is lower than 3.5V, the VREG will turn off. After a recovery time of about three milliseconds, the VREG will be checked again. If there is no short circuit, (VREG > 3.5V) then the VREG will be switched back on.

The regulator has a thermal shutdown. If the thermal protection circuit detects an over temperature condition, and the signals TXD and RXD are LOW, or TXD is HIGH, the regulator will shut down. The recovery from the thermal shutdown is equal to adequate cooling time.

FIGURE 1-4: VOLTAGE REGULATOR BLOCK DIAGRAM



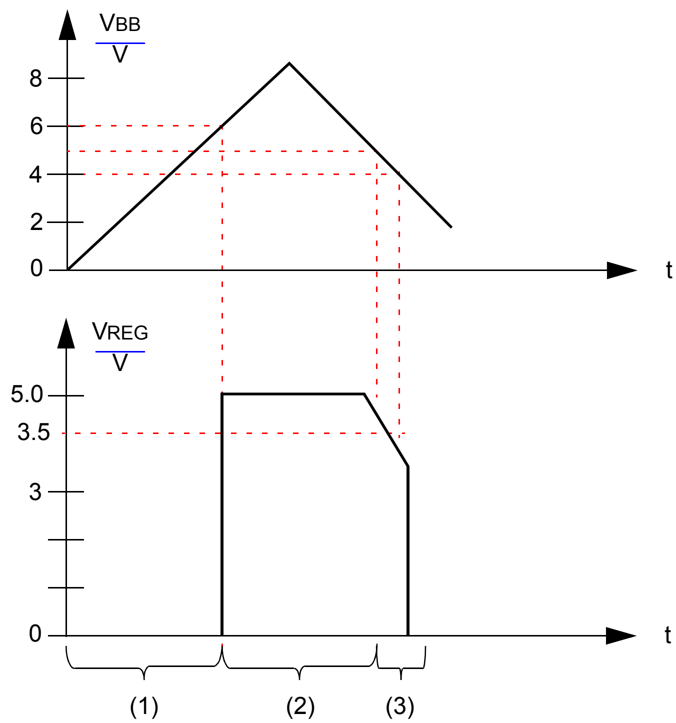
1.6.2 3.3V REGULATOR

A metal option provides for a alternate 3.30 V_{DC} ±3% at up to 50 mA of load current over the entire operating temperature range of -40°C to +125°C. All specifications given above for the 5.0V operation apply except for any difference noted here.

The same input tracking of 4.25V applies the 3.3V regulator.

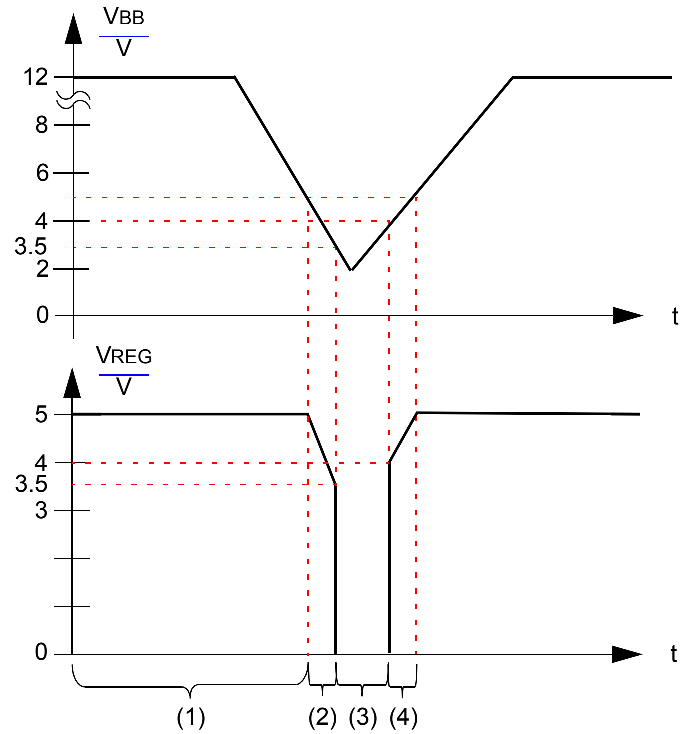
Note: The regulator has an overload current limiting of approximately 100 mA. If V_{REG} is lower than 2.5V, the V_{REG} will turn off.

FIGURE 1-5: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET



Note 1: Start-up, V_{BB} < 5.75V, regulator off.
2: V_{BB} > 5.75V, regulator on.
3: $V_{BB} \leq$ 5.5V, regulator tracks V_{BB}
4: V_{BB} < 4.25V, regulator will turn off

FIGURE 1-6: VOLTAGE REGULATOR OUTPUT ON POWER DIP



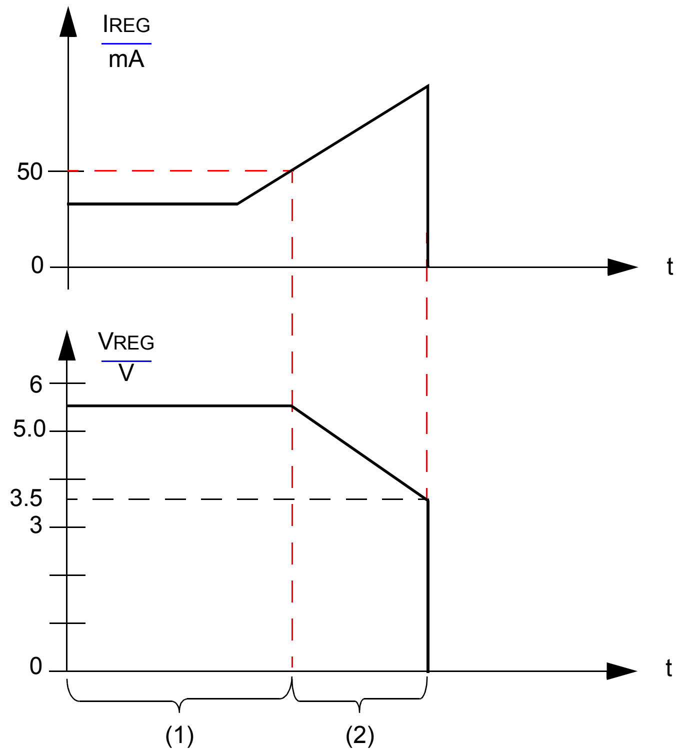
Note 1: Voltage regulator on.

2: $V_{BB} \leq 5.5V$, regulator tracks V_{BB} until $V_{BB} < 4.25V$.

3: $V_{REG} < 3.5V$, regulator is off.

4: $V_{BB} > 5.75V$, regulator on.

FIGURE 1-7: VOLTAGE REGULATOR OUTPUT ON OVERCURRENT SITUATION



Note 1: IREG less than 50 mA, regulator on.

2: After IREG exceeds IREGmax, voltage regulator output will be reduced until VREG off is reached.

1.7 ICSP™ Considerations

The following should be considered when the MCP202X is connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller should be supplied from the programmer, not from the MCP202X
- The MCP202X should be left unpowered
- The voltage on VREG should not exceed the maximum output voltage of VREG

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{IN} DC Voltage on Logic pins except CS/LWAKE .... -0.3 to V_{REG}+0.3V
V_{IN} DC Voltage on CS/LWAKE .... -0.3 to +43V
V_{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) .... -0.3 to +43V
V_{BB} Battery Voltage, transient (**Note 1**) .... -0.3 to +43V
V_{BB} Battery Voltage, continuous .... -0.3 to +30V
V_{LBUS} Bus Voltage, continuous .... -18 to +30V
V_{LBUS} Bus Voltage, transient (**Note 1**) .... -27 to +43V
I_{LBUS} Bus Short Circuit Current Limit .... 200 mA
ESD protection on LIN, V_{BB} (Human Body Model) (**Note 2**) .... >6 kV
ESD protection on all other pins (Human Body Model) (**Note 2**) .... >4 kV
Maximum Junction Temperature .... 150°C
Storage Temperature .... -55 to +150°C

Note 1: ISO 7637/1 load dump compliant (t < 500 ms).
2: According to JESD22-A114-B.

† NOTICE: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 DC Specifications

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C $C_{LOADREG}$ = 10 µF					
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power						
V_{BB} Quiescent Operating Current	I_{BBQ}		115	210	µA	I_{OUT} = 0 mA, L_{BUS} recessive
		—	120	215	µA	V_{OUT} = 3.3V
V_{BB} Transmitter-off Current	I_{BBTO}	—	90	190	µA	With V_{REG} on, transmitter off, receiver on, $\overline{FAULT}$/TXE = V_{IL}, CS = V_{IH}
		—	95	210	µA	V_{OUT} = 3.3V
V_{BB} Power-down Current	I_{BBPD}	—	16	26	µA	With V_{REG} powered-off, receiver on and transmitter off, $\overline{FAULT}$/TXE = V_{IH}, TXD = V_{IH}, CS = V_{IL})
V_{BB} Current with V_{SS} Floating	$I_{BBNOGND}$	-1	—	1	mA	V_{BB} = 12V, GND to V_{BB}, VLIN=0-18V
Microcontroller Interface						
High Level Input Voltage (TXD, $\overline{FAULT}$/TXE)	V_{IH}	2.0 or (0.25V_{REG} +0.8)	—	V_{REG} +0.3	V	
Low Level Input Voltage (TXD, $\overline{FAULT}$/TXE)	V_{IL}	-0.3	—	0.15 V_{REG}	V	
High Level Input Current (TXD)	I_{IH}	-2.5	—	-0.25	µA	Input voltage = 0.8*V_{REG}
Low Level Input Current (TXD)	I_{IL}	-10	—	-3.0	µA	Input voltage = 0.2*V_{REG}
Pull-up Current on Input (TXD)	I_{PU}TXD	0.7	—	3.0	µA	~800 kΩ internal pull-up to V_{REG} @ V_{IH} = 0.7*V_{REG}
High Level Input Voltage (CS/LWAKE)	V_{IH}	0.7V_{REG}	—	V_{BB}	V	Through a current-limiting resistor
Low Level Input Voltage (CS/LWAKE)	V_{IL}	-0.3	—	0.3V_{REG}	V	
High Level Input Current (CS/LWAKE)	I_{IH}	1.0	—	7.0	µA	Input voltage = 0.8*V_{REG}
Low Level Input Current (CS/LWAKE)	I_{IL}	0.3	—	3.0	µA	Input voltage = 0.2*V_{REG}
Pull-down Current on Input (CS/LWAKE)	I_{PDCS}	1.0	—	6.0	µA	~1.3MΩ internal pull-down to V_{SS} @ V_{IH} = 3.5V

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).

2: For design guidance only, not tested.

3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.2 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C $C_{LOADREG}$ = 10 µF					
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Bus Interface						
High Level Input Voltage	$V_{IH}(L_{BUS})$	0.6 V_{BB}	—	18	V	Recessive state
Low Level Input Voltage	$V_{IL}(L_{BUS})$	-8	—	0.4 V_{BB}	V	Dominant state
Input Hysteresis	V_{HYS}	—	—	0.175 V_{BB}	V	$V_{IH}(L_{BUS})$ - $V_{IL}(L_{BUS})$
Low Level Output Current	$I_{OL}(L_{BUS})$	40	—	200	mA	Output voltage = 0.1 V_{BB}, V_{BB} = 12V
High Level Output Current	$I_{OH}(L_{BUS})$	-20	—	20	µA	V_{BUS} >= V_{BB}, V_{BUS} < 40V
Pull-up Current on Input	$I_{PU}(L_{BUS})$	5	—	180	µA	~30 kΩ internal pull-up @ V_{IH} (L_{BUS}) = 0.7 V_{BB}
Short Circuit Current Limit	I_{SC}	50	—	200	mA	**(Note 1)**
High Level Output Voltage	$V_{OH}(L_{BUS})$	0.8 V_{BB}	—	V_{BB}	V	$V_{OH}(L_{BUS})$ must be at least 0.8 V_{BB}
Low Level Output Voltage	V_{OLLO} (L_{BUS})	0.10	—	1.2	V	V_{BB} = 7.3V @ 40 mA
Input Leakage Current (at the receiver during dominant bus level)	$I_{BUS\_PAS\_DOM}$	-1	—	—	mA	Driver off, V_{BUS} = 0V, V_{BAT} = 12V
Input Leakage Current (at the receiver during recessive bus level)	$I_{BUS\_PAS\_REC}$	—	—	20	µA	Driver off, 8V < V_{BAT} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{BAT}$
Leakage Current (disconnected from ground)	$I_{BUS\_NO\_GND}$	-1	—	+1	mA	GND_{DEVICE} = V_{BAT}, 0V < V_{BUS} < 18V, V_{BAT} = 12V
Leakage Current (disconnected from V_{BAT})	I_{BUS}	—	—	100	µA	V_{BAT} = GND, 0 < V_{BUS} < 18V, **(Note 3)**
Receiver Center Voltage	V_{BUS_CNT}	0.475 V_{BB}	0.5 V_{BB}	0.525 V_{BB}	V	V_{BUS_CNT} = V_{IL} (L_{BUS}) + V_{IH} (L_{BUS})/2
Slave Termination	Rslave	20	30	47	kΩ	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).
2: For design guidance only, not tested.
3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.2 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C $C_{LOADREG}$ = 10 µF					
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Voltage Regulator - 5.0V						
Output Voltage	V_{OUT}	4.85	5.00	5.15	V	0 mA < I_{OUT} < 50 mA, 5.5V < V_{BB} < 18V
Load Regulation	$\Delta V_{OUT}2$	—	10	50	mV	5 mA < I_{OUT} < 50 mA refer to **Section 1.6 "Internal Voltage Regulator"**
Quiescent Current	I_{VRQ}	—	—	25	µA	I_{OUT} = 0 mA, **(Note 2)**
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @10-20 kHz C_{LOAD} = 10 µf, I_{LOAD} = 50 mA
Output Noise Voltage	eN	—	—	100	µV_{RMS}	10 Hz – 40 MHz C_{FILTER} = 10 µf, C_{BP} = 0.1 µf, C_{LOAD} 10 µf, I_{LOAD} = 50 mA
Shutdown Voltage	V_{SD}	3.5	—	4.0	V	See Figure 1-5
Input Voltage to Maintain Regulation	V_{BB}	5.5	—	18.0	V	
Input Voltage to Turn Off Output	V_{OFF}	4.0	—	4.5	V	
Input Voltage to Turn On Output	V_{ON}	5.5	—	6.0	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).
2: For design guidance only, not tested.
3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.2 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C $C_{LOADREG}$ = 10 µF					
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Voltage Regulator - 3.3V						
Output Voltage	V_{OUT}	3.20	3.30	3.40	V	0 mA < I_{OUT} < 50 mA, 5.5V < V_{BB} < 18V
Line Regulation	ΔV_{OUT1}	—	10	50	mV	I_{OUT} = 1 mA, 6.0V < V_{BB} < 18V
Load Regulation	ΔV_{OUT2}	—	10	50	mV	5 mA < I_{OUT} < 50 mA Refer to **Section 1.6 "Internal Voltage Regulator"**
Quiescent Current	I_{VRQ}	—	—	25	µA	I_{OUT} = 0 mA, **(Note 2)**
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @10-20 kHz C_{LOAD} = 10 µf, I_{LOAD} = 50 mA
Output Noise Voltage	eN	—	—	100	$\mu V_{RMS}/\sqrt{Hz}$	10 Hz – 40 MHz C_{FILTER} = 10 µf, C_{BP} = 0.1 µf C_{LOAD} = 10 µf, I_{LOAD} = 50 mA
Shutdown Voltage	V_{SD}	2.5	—	2.7	V	See Figure 1-5
Input Voltage to Maintain Regulation	V_{BB}	5.5	—	V_{BB} = 18.0	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).

2: For design guidance only, not tested.

3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.3 AC Specification

AC CHARACTERISTICS	V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Bus Interface - Constant Slope Time Parameters						
Slope rising and falling edges	t_{SLOPE}	3.5	—	22.5	µs	7.3V <= V_{BB} <= 18V
Symmetry of Propagation Delay of Transmitter rising edge w.r.t. falling edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{TRANSPDR}$), V_{BB} = 7.3V
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	4.0	µs	$t_{TRANSPD}$ = max ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	µs	t_{RECPD} = max (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver rising edge w.r.t. falling edge	t_{RECSYM}	-2.0	—	2.0	µs	t_{RECSYM} = max (t_{RECPDF} - t_{RECPDR})
Symmetry of Propagation Delay of Transmitter rising edge w.r.t. falling edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{TRANSPDR}$)
Time to sample of FAULT/TXE for bus conflict reporting	t_{FAULT}	—	—	32.5	µs	t_{FAULT} = max ($t_{TRANSPD}$ + t_{SLOPE} + t_{RECPD})
Duty Cycle 1 @20.0kbit/sec		39.6	—	—	$\%t_{BIT}$	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.744 x V_{BB}, $TH_{DOM(MAX)}$ = 0.581 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 50 µs. D1 = $t_{BUS\_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 2 @20.0kbit/sec		—	—	58.1	$\%t_{BIT}$	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.284 x V_{BB}, $TH_{DOM(MAX)}$ = 0.422 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 50 µs. D2 = $t_{BUS\_REC(MAX)}$ / 2 x t_{BIT})
Duty Cycle 3 @10.4kbit/sec		40.1	—	—	$\%t_{BIT}$	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.778 x V_{BB}, $TH_{DOM(MAX)}$ = 0.616 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 96 µs. D3 = $t_{BUS\_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 4 @10.4kbit/sec		—	—	56.6	$\%t_{BIT}$	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.251 x V_{BB}, $TH_{DOM(MAX)}$ = 0.389 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 96 µs. D4 = $t_{BUS\_REC(MAX)}$ / 2 x t_{BIT})

AC CHARACTERISTICS	V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Voltage Regulator						
Bus Activity Debounce time	t_{BDB}	5	10	20	µs	Bus debounce time
Bus Activity to Voltage Regulator Enabled	t_{BACTVE}	35	52	100	µs	After Bus debounce time
Voltage Regulator Enabled to Ready	t_{VEVR}	300	—	1200	µs	**(Note 1)**
Chip Select to Operation Ready	t_{CSOR}	**TBD**	—	300	µs	**(Note 1)**
Chip Select to Power-down	t_{CSPD}	**TBD**	—	40	µs	
Short circuit to shut-down	$t_{SHUTDOWN}$	20	—	100	µs	
$\overline{\text{RESET}}$ Timing						
V_{REG} OK detect to $\overline{\text{RESET}}$ inactive	t_{RPU}	—	—	10.0	µs	
V_{REG} OK detect to $\overline{\text{RESET}}$ active	t_{RPD}	—	—	10.0	µs	

Note 1: Time depends on external capacitance and load.

2.4 Thermal Specifications

THERMAL CHARACTERISTICS					
Parameter	**Symbol**	**Typ**	**Max**	**Units**	**Test Conditions**
Recovery Temperature	$\theta_{RECOVERY}$	+140	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	+150	—	°C	
Short Circuit Recovery Time	t_{THERM}	1.5	5.0	ms	

Note 1: The maximum power dissipation is a function of T_{JMAX}, Θ_{JA} and ambient temperature T_A. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A)\Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP2021 will go into thermal shutdown.

2.5 Timing Diagrams and Specifications

FIGURE 2-1: BUS TIMING DIAGRAM

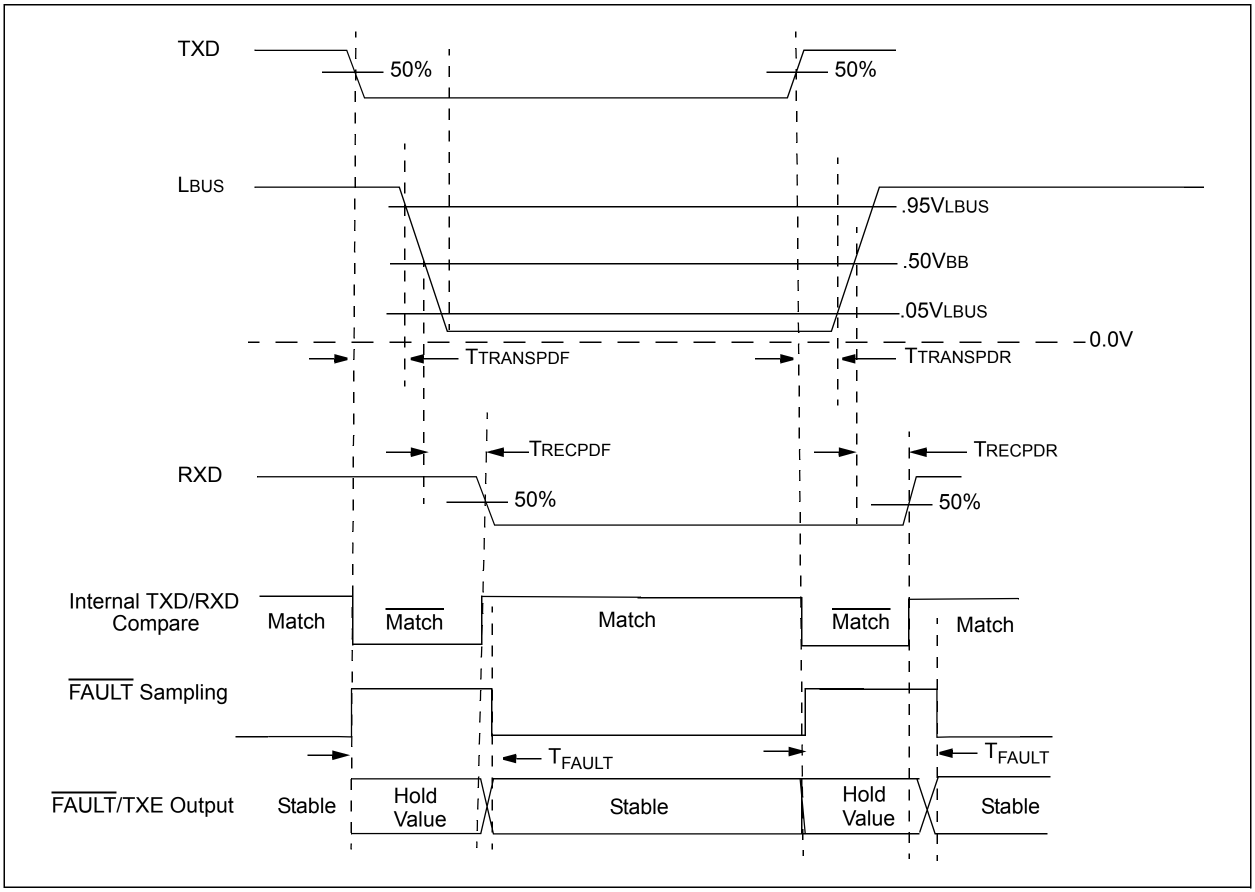


FIGURE 2-2: REGULATOR CS/LWAKE TIMING DIAGRAM

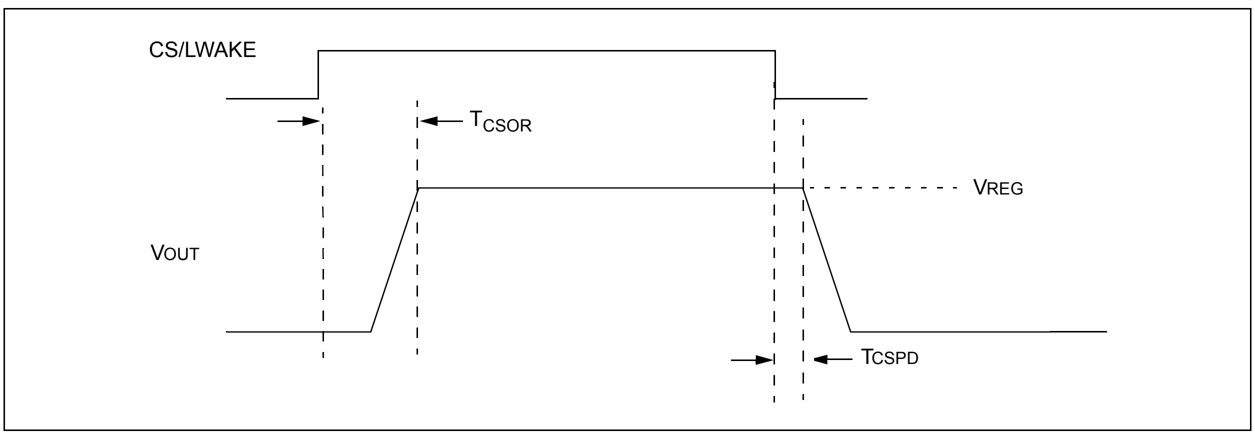


FIGURE 2-3: REGULATOR BUS WAKE TIMING DIAGRAM

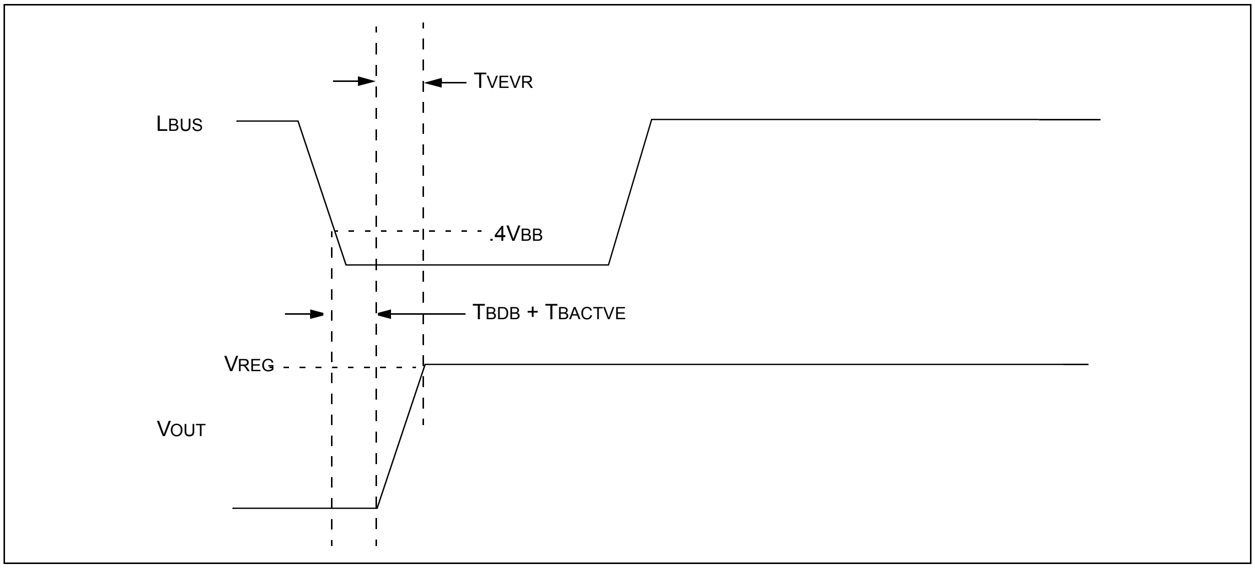


FIGURE 2-4: $\overline{\text{RESET}}$ TIMING DIAGRAM

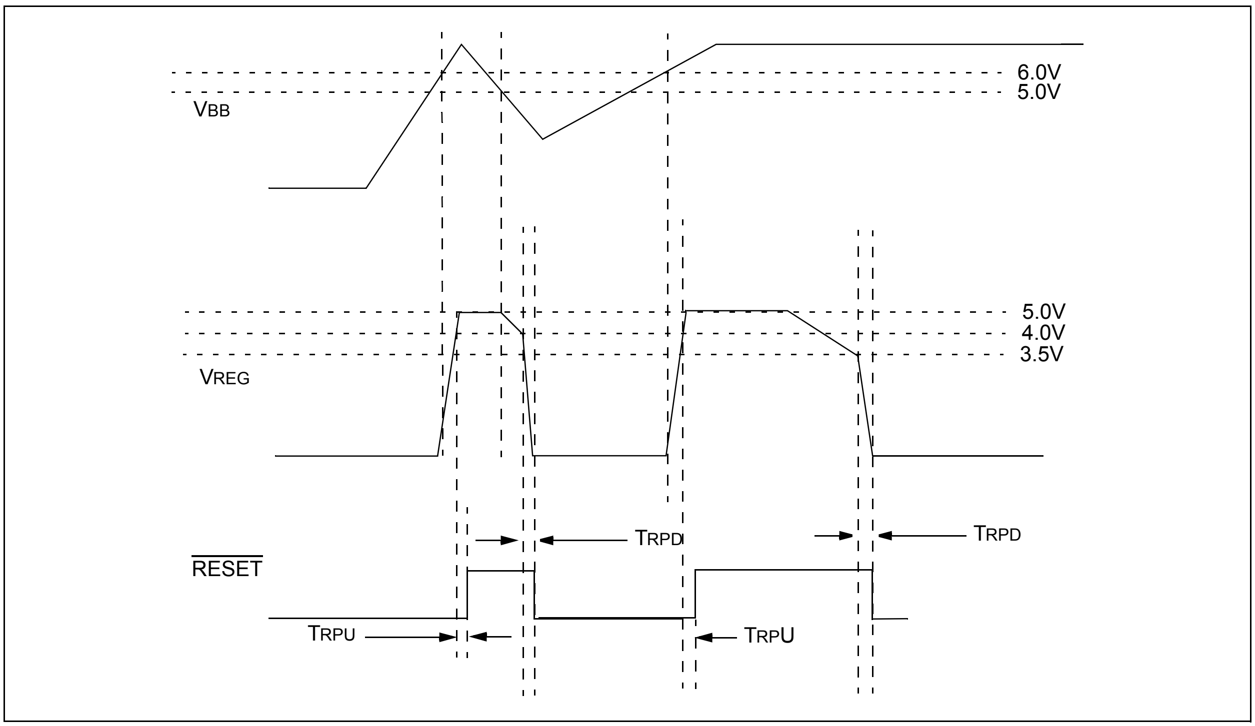
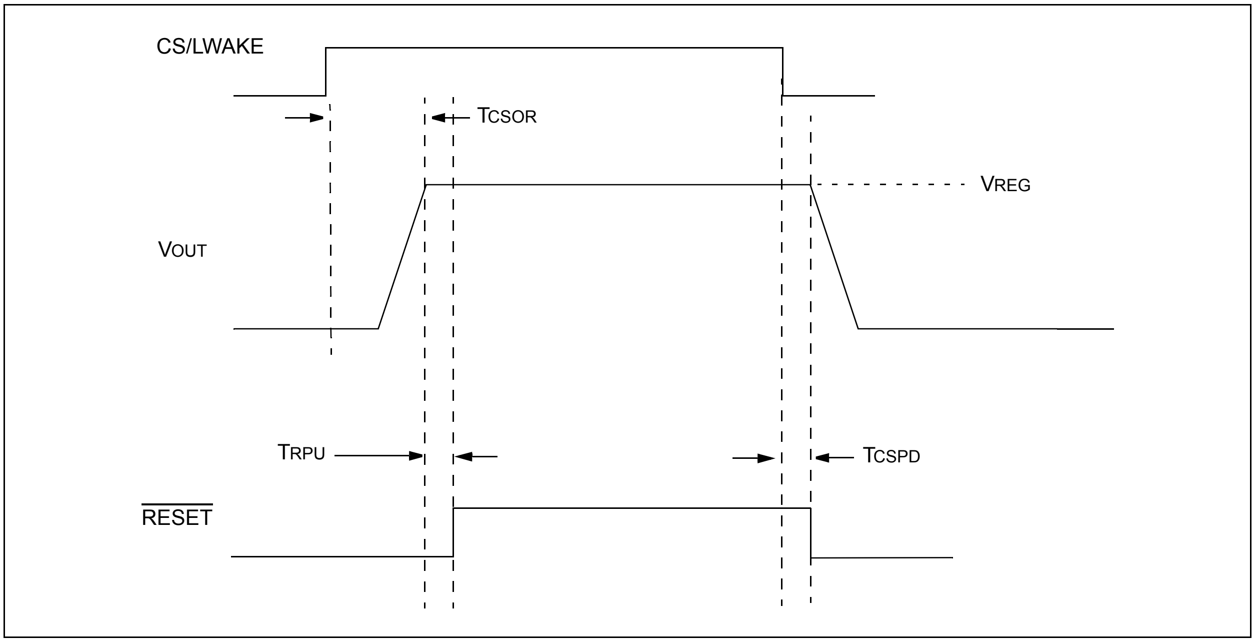


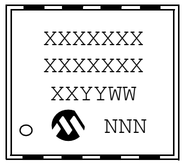
FIGURE 2-5: CS/LWAKE TO $\overline{\text{RESET}}$ TIMING DIAGRAM



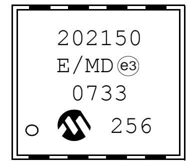
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

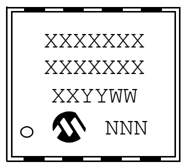
8-Lead DFN (4x4)



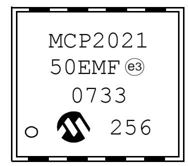
Example:



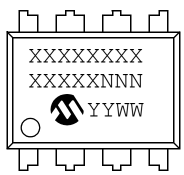
8-Lead DFN-S (6x5)



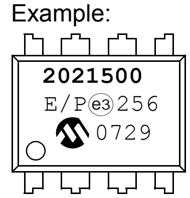
Example:



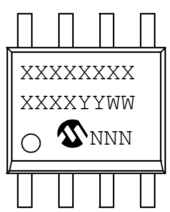
8-Lead PDIP (300 mil)



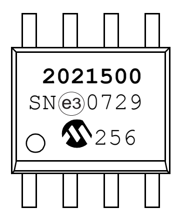
Example:



8-Lead SOIC (150 mil)



Example:

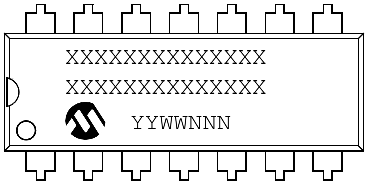


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

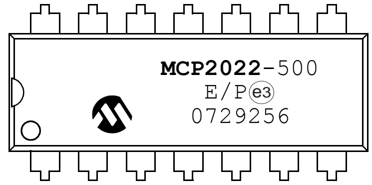
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3.1 Package Marking Information (Continued)

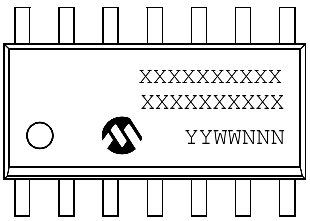
14-Lead PDIP (300 mil) **(MCP2022)**



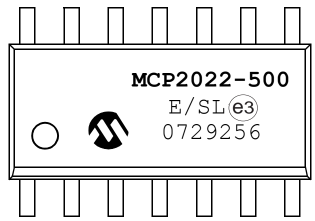
Example:



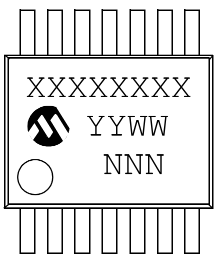
14-Lead SOIC (150 mil) **(MCP2022)**



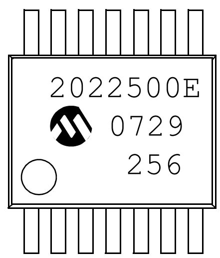
Example:



14-Lead TSSOP (**MCP2022**)



Example

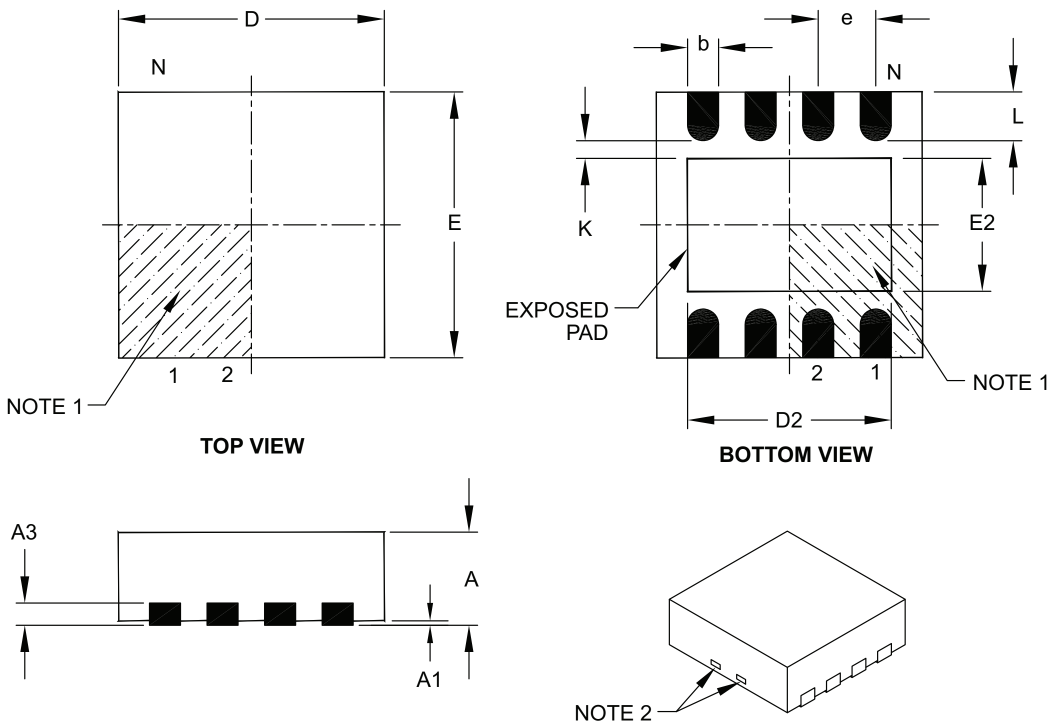


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	0.00	2.20	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	0.00	3.00	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.55	0.65
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

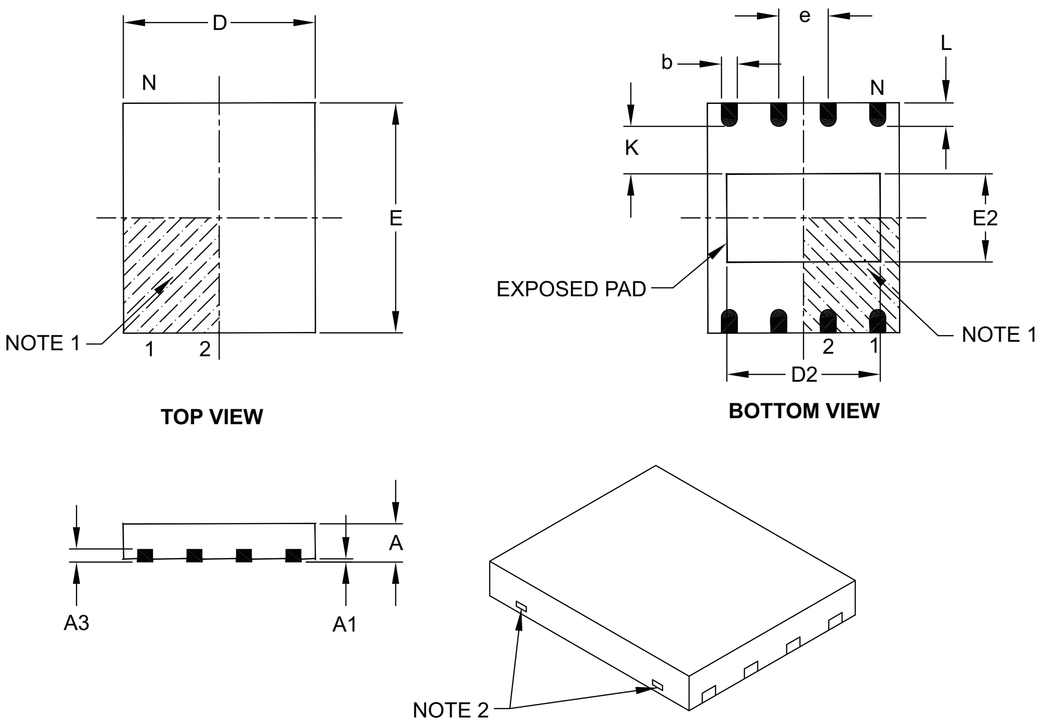
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

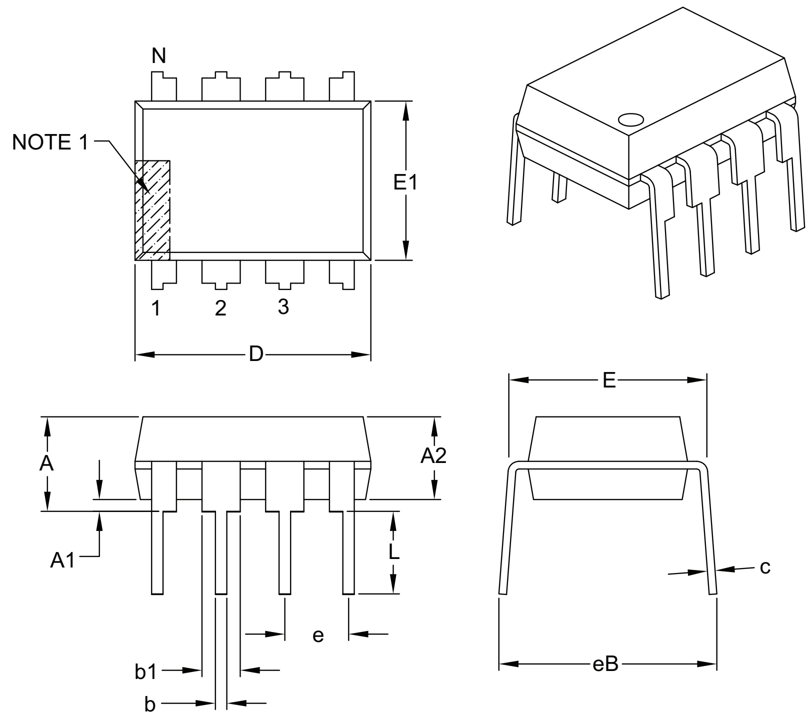
Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122B

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



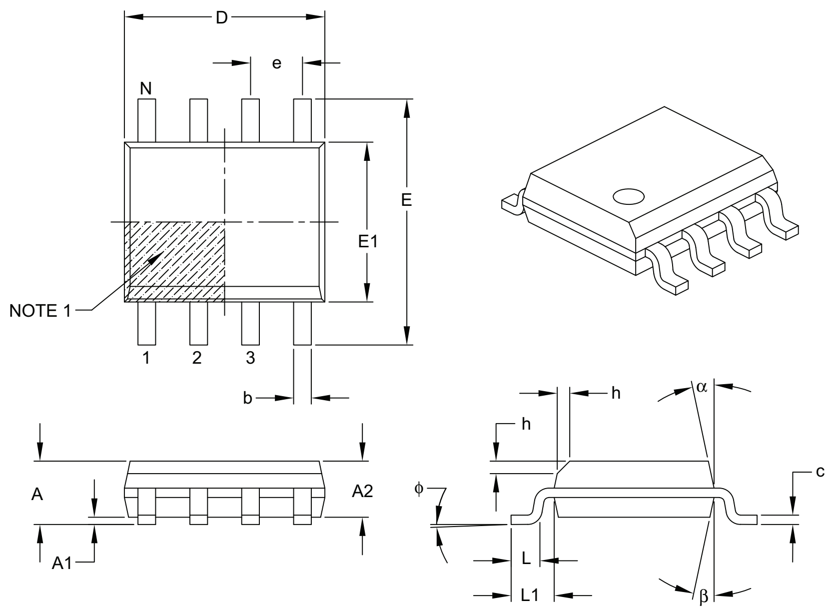
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

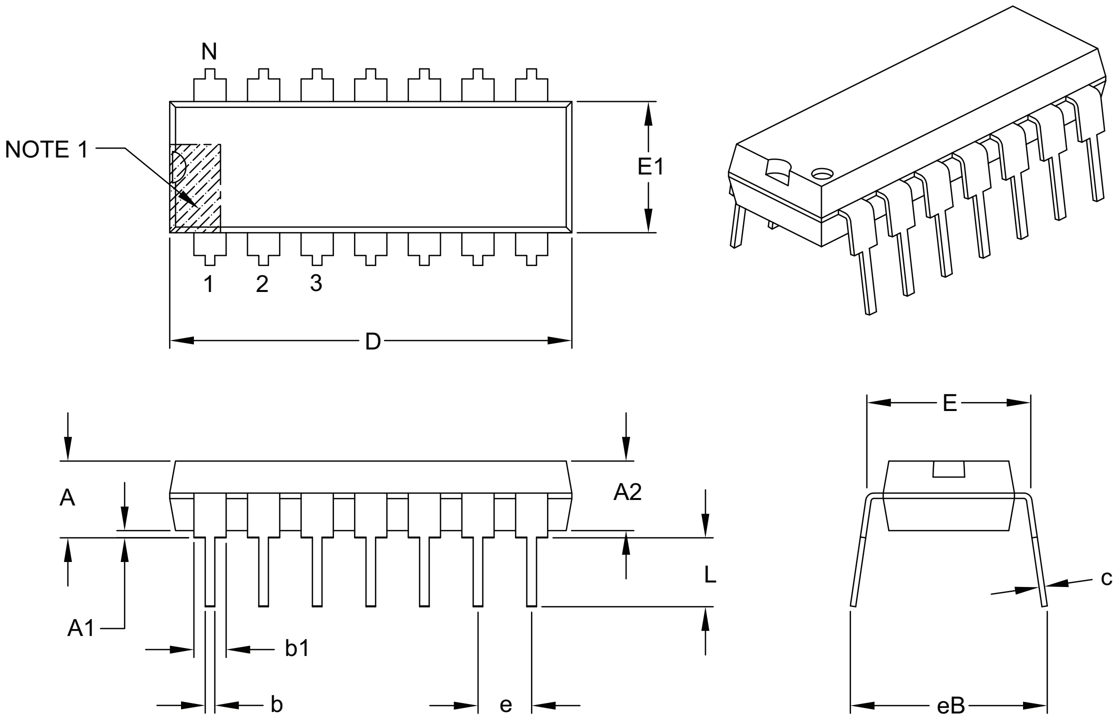
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

 Preliminary

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

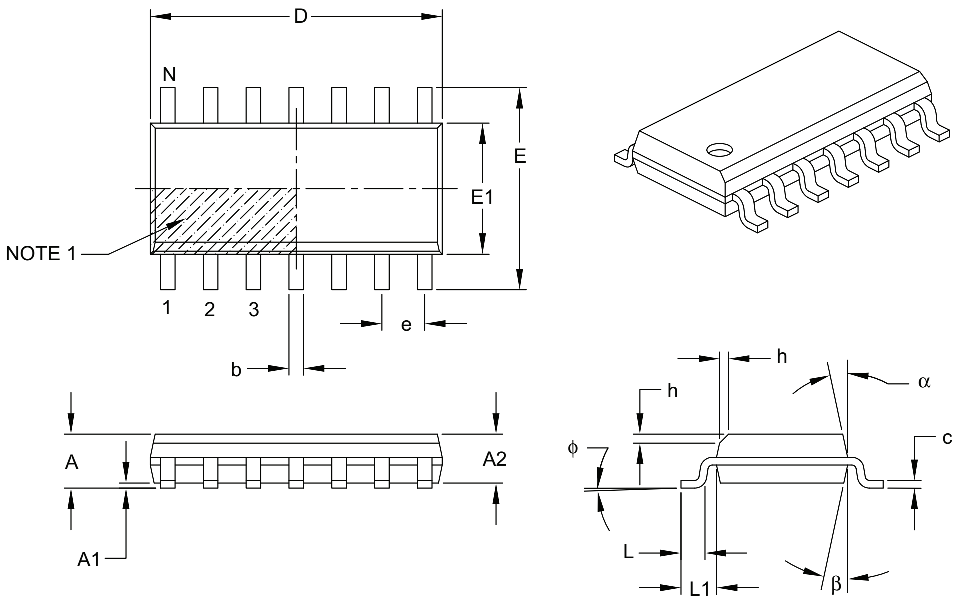
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

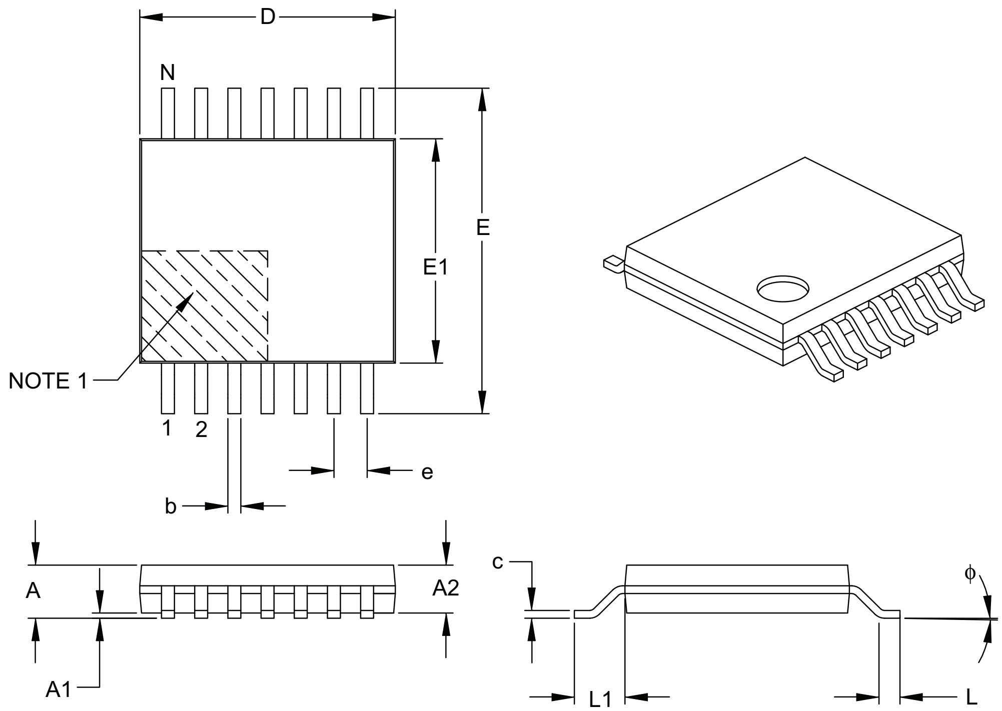
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

 Preliminary

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N			14	
Pitch	e			0.65 BSC	
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.80	1.00	1.05
Standoff	A1		0.05	–	0.15
Overall Width	E			6.40 BSC	
Molded Package Width	E1		4.30	4.40	4.50
Molded Package Length	D		4.90	5.00	5.10
Foot Length	L		0.45	0.60	0.75
Footprint	L1			1.00 REF	
Foot Angle	ϕ		0°	–	8°
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (August 2007)

1. Modified Block Diagram on page 2.
2. **Section 1.3.5 “Transmitter OFF Mode”**: Deleted text in 1st paragraph.
3. **Example 1-1**: Removed +5V notation.
4. **Section 1.5 “Pin Descriptions”**: Removed 10-pin DFN, MSOP column from table.
5. **Section 1.5.8 “Fault/TXE”**: Deleted text from 2nd paragraph.
6. **Section 3.0 “Packaging Information”**: Added 8-lead 4x4 and 6x5 DFN and 14-lead TSSOP packages. Updated package outline drawings and added drawings for 8-lead DFN and 14-lead TSSOP drawings.

Revision A (November 2005)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XX
Device	Temperature Range	Package

Device:	MCP2021:	LIN Transceiver with Voltage Regulator
	MCP2021T:	LIN Transceiver with Voltage Regulator (Tape and Reel) (SOIC only)
	MCP2022:	LIN Transceiver with Voltage Regulator
	MCP2022T:	LIN Transceiver with Voltage Regulator (Tape and Reel) (SOIC only)
Temperature Range:	E	= -40°C to +125°C
Package:	MD	= Plastic Micro Small Outline (4x4), 8-lead
	MF	= Plastic Micro Small Outline (6x5), 8-lead
	P	= Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN	= Plastic SOIC, (150 mil Body), 8-lead
	SL	= Plastic SOIC, (150 mil Body), 14-lead
	ST	= Plastic Thin Shrink Small Outline, 14-lead

Examples:

a) MCP2021-330E/SN: 3.3V, 8L-SOIC pkg.
b) MCP2021-330E/P: 3.3V, 8L-PDIP pkg.
c) MCP2021-500E/MF: 5.0V, 8L-DFN-S pkg.
d) MCP2021-500E/SN: 5.0V, 8L-SOIC pkg.
e) MCP2021-500E/MD: 5.0V, 8L-DFN pkg.
f) MCP2021-330E/P: 5.0V, 8L-PDIP pkg.
g) MCP2021T-330E/SN: Tape and Reel, 3.3V, 8L-SOIC pkg.
h) MCP2021T-500E/MD: Tape and Reel, 5.0V, 8L-DFN pkg.
i) MCP2021T-500E/SN: Tape and Reel, 5.0V, 8L-SOIC pkg.

a) MCP2022-330E/SN: 3.3V, 14L-SOIC pkg.
b) MCP2022-330E/P: 3.3V, 14L-PDIP pkg.
c) MCP2022-500E/SN: 5.0V, 14L-SOIC pkg.
d) MCP2022-500E/P: 5.0V, 14L-PDIP pkg.
e) MCP2022T-330E/SN: Tape and Reel, 3.3V, 14L-SOIC pkg.
f) MCP2022T-500E/SN: Tape and Reel, 5.0V, 14L-SOIC pkg.
g) MCP2022T-500E/ST: Tape and Reel, 5.0V, 14L-TSSOP pkg.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

SALES AND SERVICE

HY-LINE®
POWER COMPONENTS

Inselkammerstraße 10	Gründenstrasse 10
D-82008 Unterhaching	CH-8247 Flurlingen
Tel.: +49 (0)89 614503 10	Tel.: +41 (0)52 647 42 00
Fax: +49 (0)89 614503 20	Fax: +41 (0)52 647 42 01
E-Mail: power@hy-line.de	E-Mail: power@hy-line.ch
URL: www.hy-line.de	URL: www.hy-line.ch

06/25/07