

## Errata for DS\_INAP\_125R, Rev 1.3

Order ID:  
ER\_INAP125R\_1\_3  
August 2009  
Revision 1.0

### Scope

The errata below describe situations, in which the INAP125R does not perform according to the datasheet. The sections below shall replace the original sections of the datasheet.

### Section 3.2 "Reset"

The Reset pin triggers an asynchronous reset (active low) which can be activated at any time and sets the INAP125T/24 into a defined state. The minimum low pulse width is four reference clock cycles.

During reset the serial output pins SDOUT-, SDOUT+ are held on VDDA level. PX\_CLK, SBDOWN\_DATA[1:0] and SBDOWN\_CLK are at low level. EEPROM\_DATA is high impedance.

The parallel pixel data interface PX\_DATA[23:0] only applies valid data with pixel clock available at PX\_CLK. During reset, PX\_DATA[23:0] hold the last status which was present before reset.

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