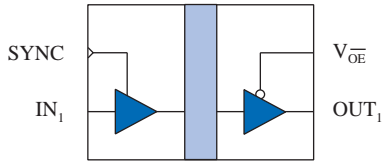
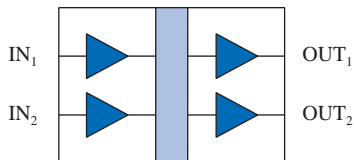


## 2 Mbps DC-Correct Digital Isolators

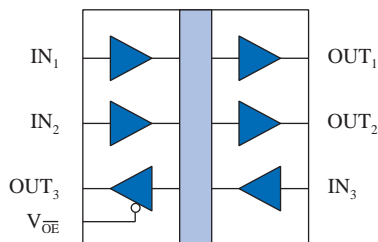
### Functional Diagrams



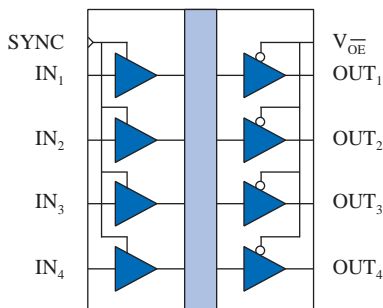
**IL510**



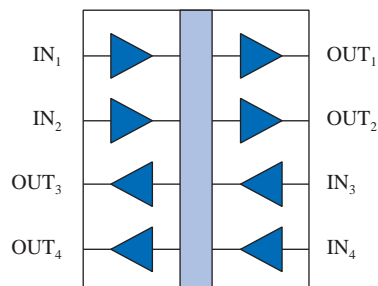
**IL511**



**IL514**



**IL515**



**IL516**

IsoLoop is a registered trademark of NVE Corporation.  
\*U.S. Patent numbers 5,831,426; 6,300,617 and others.

### Features

- +5 V / +3.3 V CMOS/TTL Compatible
- 2 Mbps Maximum Speed
- DC-Correct
- External Clocking Option (IL510 and IL515)
- Very Low EMC
- 2500 V<sub>RMS</sub> Isolation (1 min.)
- 10 ns Pulse Width Distortion
- 25 ns Propagation Delay
- 30 kV/μs Typical Common Mode Rejection
- Low EMC Footprint
- 8-pin MSOP; 0.3" and 0.15" 8-pin and 16-pin SOIC Packages
- UL 1577 and IEC 61010-2001 Approved

### Applications

- ADCs and DACs
- Digital Fieldbus
- RS-485 and RS-422
- Multiplexed Data Transmission
- Data Interfaces
- Board-to-Board Communication
- Hi-Fi Audio
- Digital Noise Reduction
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting

### Description

NVE's IL500-Series isolators are CMOS devices manufactured with NVE's patented\* IsoLoop<sup>®</sup> spintronic Giant Magnetoresistive (GMR) technology.

Compared to the industry-standard IL700-Series isolators, which have speeds up to 150 Mbps, IL500-Series isolators are more cost effective, offer a DC-correct design, and have an external clocking option on some models.

All IL500-Series isolator channels operate at 2 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a propagation delay of 25 ns and a pulse width distortion of 10 ns.

Ihr Vertriebspartner:  
**HY-LINE**<sup>®</sup>  
POWER COMPONENTS

Inselkammerstraße 10  
D-82008 Unterhaching  
Tel.: +49 (0)89 614503 10  
Fax: +49 (0)89 614503 20  
E-Mail: power@hy-line.de  
URL: www.hy-line.de

Gründenstrasse 10  
CH-8247 Flurlingen  
Tel.: +41 (0)52 647 42 00  
Fax: +41 (0)52 647 42 01  
E-Mail: power@hy-line.ch  
URL: www.hy-line.ch

**REV. F**

## Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	$T_S$	-55		150	°C	
Ambient Operating Temperature <sup>(1)</sup>	$T_A$	-55		150	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	-0.5		7	V	
Input Voltage	$V_I$	-0.5		$V_{DD}+0.5$	V	
Output Voltage	$V_O$	-0.5		$V_{DD}+0.5$	V	
Output Current Drive	$I_O$			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

## Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	$T_A$	-40		85	°C	
Supply Voltage	$V_{DD1}, V_{DD2}$	3.0		5.5	V	
Logic High Input Voltage	$V_{IH}$	2.4		$V_{DD}$	V	
Logic Low Input Voltage	$V_{IL}$	0		0.8	V	
Input Signal Rise and Fall Times <sup>(10)</sup>	$t_{IR}, t_{IF}$		DC-Correct			

## Insulation Specifications

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance						
MSOP		3.0			mm	
0.15" SOIC (8-pin or 16-pin)		4.0			mm	
0.3" SOIC		8.1			mm	
Leakage Current			0.2		μA	240 V <sub>RMS</sub> , 60 Hz
Barrier Impedance			$>10^{14}  3$		Ω    pF	

## Package Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Capacitance (Input-Output) <sup>(5)</sup>	$C_{I-O}$		4		pF	f = 1 MHz
Thermal Resistance						
MSOP	$\theta_{JC}$		168		°C/W	Thermocouple at center underside of package
0.15" 8-pin SOIC	$\theta_{JC}$		144		°C/W	
0.15" 16-pin SOIC	$\theta_{JC}$		41		°C/W	
0.3" 16-pin SOIC	$\theta_{JC}$		28		°C/W	
Package Power Dissipation	$P_{PD}$			150	mW	f = 1 MHz, $V_{DD} = 5$ V

## Safety and Approvals

### IEC61010-1

TUV Certificate Numbers: **N1502812, N1502812-101**

### Classification as Reinforced Insulation

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL5xx-1	MSOP	II	III	150 V <sub>RMS</sub>
IL5xx-3	8-pin and 16-pin 0.15" SOIC	II	III	150 V <sub>RMS</sub>
IL5xx	0.3" SOIC	II	III	300 V <sub>RMS</sub>

### UL 1577

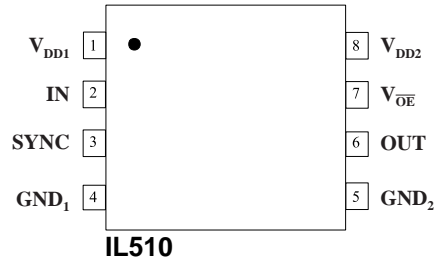
Component Recognition Program File Number: E207481  
 Rated 2500V<sub>RMS</sub> for 1 minute

### Soldering Profile

Per JEDEC J-STD-020C, MSL=2

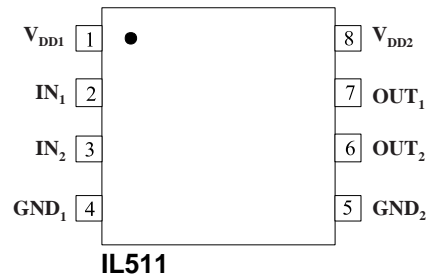
## IL510 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	IN	Data In
3	SYNC	External clock
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	OUT	Data Out
7	V <sub>OE</sub>	Output enable (internally held low with 100 kΩ)
8	V <sub>DD2</sub>	Supply voltage



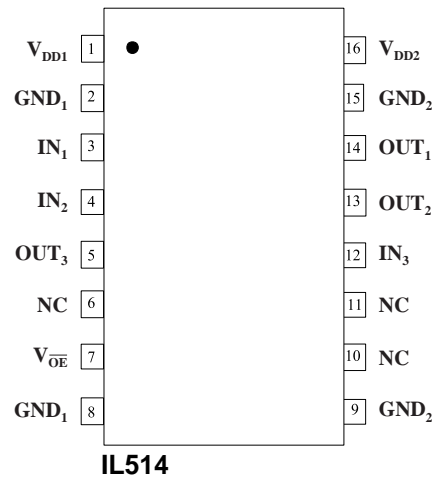
## IL511 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	IN <sub>1</sub>	Data in, channel 1
3	IN <sub>2</sub>	Data in, channel 2
4	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
5	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
6	OUT <sub>2</sub>	Data out, channel 2
7	OUT <sub>1</sub>	Data out, channel 1
8	V <sub>DD2</sub>	Supply voltage



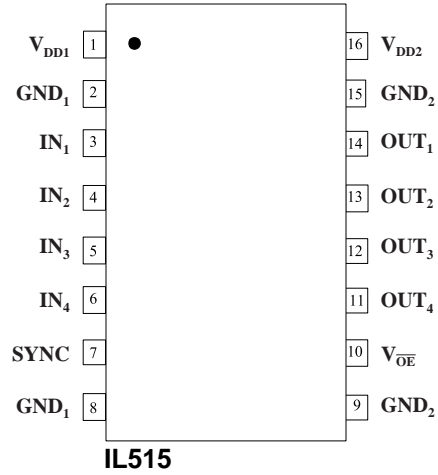
## IL514 Pin Connections

1	V <sub>DD1</sub>	Supply Voltage 1
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (internally connected to pin 8)
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	OUT <sub>3</sub>	Data out, channel 3
6	NC	No connection
7	V <sub>OE</sub>	Output enable, channel 3 (internally held low with 100 kΩ)
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub> (internally connected to pin 2)
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (internally connected to pin 15)
10	NC	No Connection
11	NC	No Connection
12	IN <sub>3</sub>	Data in, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub> (internally connected to pin 9)
16	V <sub>DD2</sub>	Supply voltage



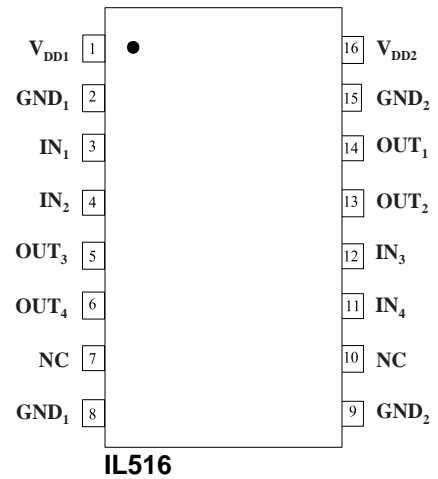
## IL515 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	IN <sub>3</sub>	Data in, channel 3
6	IN <sub>4</sub>	Data in, channel 4
7	SYNC	External clock
8	GND <sub>1</sub>	Ground return for V <sub>DD1</sub>
9	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
10	V <sub>OE</sub>	Output enable (internally held low with 100 kΩ)
11	OUT <sub>4</sub>	Data out, channel 4
12	OUT <sub>3</sub>	Data out, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground return for V <sub>DD2</sub>
16	V <sub>DD2</sub>	Supply voltage

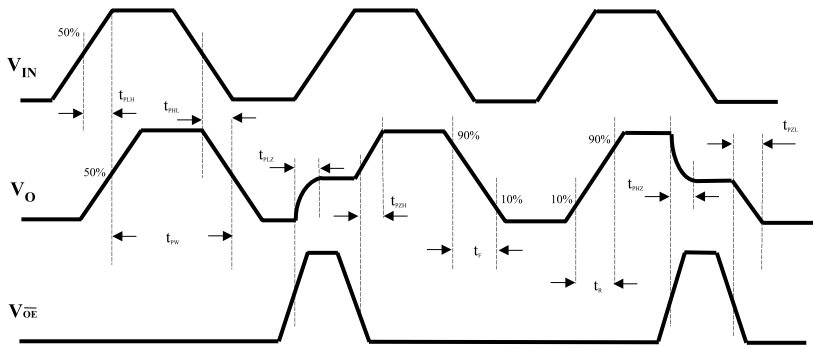


## IL516 Pin Connections

1	V <sub>DD1</sub>	Supply voltage
2	GND <sub>1</sub>	Ground Return for V <sub>DD1</sub>
3	IN <sub>1</sub>	Data in, channel 1
4	IN <sub>2</sub>	Data in, channel 2
5	OUT <sub>3</sub>	Data out, channel 3
6	OUT <sub>4</sub>	Data out, channel 4
7	NC	No connection
8	GND <sub>1</sub>	Ground Return for V <sub>DD1</sub>
9	GND <sub>2</sub>	Ground Return for V <sub>DD2</sub>
10	NC	No connection
11	IN <sub>4</sub>	Data in, channel 4
12	IN <sub>3</sub>	Data in, channel 3
13	OUT <sub>2</sub>	Data out, channel 2
14	OUT <sub>1</sub>	Data out, channel 1
15	GND <sub>2</sub>	Ground Return for V <sub>DD2</sub>
16	V <sub>DD2</sub>	Supply voltage

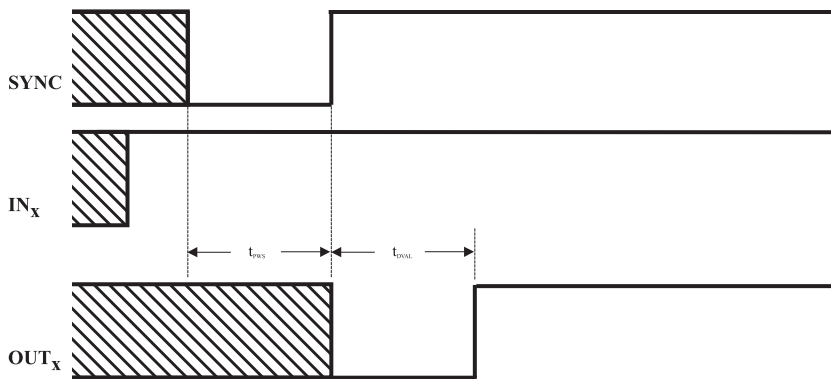


## Timing Diagrams



### Legend

$t_{PLH}$	Propagation Delay, Low to High
$t_{PHL}$	Propagation Delay, High to Low
$t_{PW}$	Minimum Pulse Width
$t_{PLZ}$	Propagation Delay, Low to High Impedance
$t_{PZH}$	Propagation Delay, High Impedance to High
$t_{PHZ}$	Propagation Delay, High to High Impedance
$t_{PZL}$	Propagation Delay, High Impedance to Low
$t_R$	Rise Time
$t_F$	Fall Time



### Legend

$t_{PWS}$	SYNC Pulse Width
$t_{DVAL}$	Time Until Data Valid

## Truth Tables

### Output Enable

$V_I$	$V_{OE}$	$V_O$
L	L	L
H	L	H
L	H	Z
H	H	Z

### SYNC

SYNC	Function
0	Internal Refresh On
1	Internal Refresh Off
$\overline{\text{f}}$	Input Data Latched to Output

**Note:** SYNC should be connected to GND to enable internal refresh,  $V_{DD}$  to disable internal refresh, or to an external clock. The SYNC pin should not be left unconnected.

## 3.3 Volt Electrical Specifications

Electrical specifications are  $T_{min}$  to  $T_{max}$  unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
<b>DC Specifications</b>						
Input Quiescent Supply Current						
IL510, IL511, IL515	I <sub>DD1</sub>		15	30	μA	
IL514			1.7	2	mA	
IL516			3.3	4	mA	
Output Quiescent Supply Current						
IL510	I <sub>DD2</sub>		1.7	2	mA	
IL511, IL514, IL516			3.3	4	mA	
IL515			6.6	8	mA	
Logic Input Current	I <sub>I</sub>	-10		10	μA	
Logic High Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> - 0.1	V <sub>DD</sub>		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub>
		0.8 x V <sub>DD</sub>	0.9 x V <sub>DD</sub>			I <sub>O</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.5	0.8		I <sub>O</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>
<b>Switching Specifications</b>						
Maximum Data Rate		2			Mbps	C <sub>L</sub> = 15 pF
Pulse Width <sup>(7)</sup>	PW	20			ns	V <sub>O</sub> 50% points; SYNC=0
		25			ns	V <sub>O</sub> 50% points; SYNC=1
Propagation Delay Input to Output (High to Low)	t <sub>PHL</sub>			25	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)	t <sub>PLH</sub>			25	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t <sub>PHZ</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t <sub>PLZ</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t <sub>PZH</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t <sub>PZL</sub>			5	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion <sup>(2)</sup>	PWD			10	ns	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>	t <sub>PSK</sub>			10	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%–90%)	t <sub>R</sub>		1	3	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%–90%)	t <sub>F</sub>		1	3	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	CM <sub>H</sub>  ,  CM <sub>L</sub>	20	30		kV/μs	V <sub>CM</sub> = 300 V
Channel-to-Channel Skew	t <sub>CSK</sub>		3	5	ns	C <sub>L</sub> = 15 pF
SYNC Timing						
SYNC Time Until Data Valid	t <sub>DVAL</sub>			9	μs	
Internal Clock Off Time <sup>(11)</sup>	t <sub>OFF</sub>			5	ns	
SYNC Pulse Width	t <sub>PWS</sub>	10			μs	
Internal Clock Pulse Width	t <sub>PWI</sub>	3.5		5	ns	
Dynamic Power Consumption <sup>(6)</sup>			140	240	μA/MHz	per channel
<b>Magnetic Field Immunity<sup>(8)</sup> (V<sub>DD2</sub> = 3V, 3V &lt; V<sub>DD1</sub> &lt; 5.5V)</b>						
Power Frequency Magnetic Immunity	H <sub>PF</sub>	1000	1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>	1800	2000		A/m	t <sub>p</sub> = 8μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>	1800	2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	K <sub>X</sub>		2.5			

## 5 Volt Electrical Specifications

Electrical specifications are  $T_{min}$  to  $T_{max}$  unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
<b>DC Specifications</b>						
Input Quiescent Supply Current						
IL510, IL511, IL515	I <sub>DD1</sub>		24	40	μA	
IL514			2	3	mA	
IL516			5	6	mA	
Output Quiescent Supply Current						
IL510	I <sub>DD2</sub>		2	3	mA	
IL511, IL514, IL516			4	6	mA	
IL515			9	12	mA	
Logic Input Current	I <sub>I</sub>	-10		10	μA	
Logic High Output Voltage	V <sub>OH</sub>	$V_{DD} - 0.1$	$V_{DD}$		V	I <sub>O</sub> = -20 μA, V <sub>I</sub> = V <sub>IH</sub>
		$0.8 \times V_{DD}$	$0.9 \times V_{DD}$			I <sub>O</sub> = -4 mA, V <sub>I</sub> = V <sub>IH</sub>
Logic Low Output Voltage	V <sub>OL</sub>		0	0.1	V	I <sub>O</sub> = 20 μA, V <sub>I</sub> = V <sub>IL</sub>
			0.5	0.8		I <sub>O</sub> = 4 mA, V <sub>I</sub> = V <sub>IL</sub>
<b>Switching Specifications</b>						
Maximum Data Rate		2			Mbps	C <sub>L</sub> = 15 pF
Pulse Width <sup>(7)</sup>	PW	20			ns	V <sub>O</sub> 50% points; SYNC=0
		25			ns	V <sub>O</sub> 50% points; SYNC=1
Propagation Delay Input to Output (High to Low)	t <sub>PHL</sub>			25	ns	C <sub>L</sub> = 15 pF
Propagation Delay Input to Output (Low to High)	t <sub>PLH</sub>			25	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t <sub>PHZ</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t <sub>PLZ</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t <sub>PZH</sub>			5	ns	C <sub>L</sub> = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t <sub>PZL</sub>			5	ns	C <sub>L</sub> = 15 pF
Pulse Width Distortion <sup>(2)</sup>	PWD			10	ns	C <sub>L</sub> = 15 pF
Propagation Delay Skew <sup>(3)</sup>	t <sub>PSK</sub>			10	ns	C <sub>L</sub> = 15 pF
Output Rise Time (10%–90%)	t <sub>R</sub>		1	3	ns	C <sub>L</sub> = 15 pF
Output Fall Time (10%–90%)	t <sub>F</sub>		1	3	ns	C <sub>L</sub> = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low) <sup>(4)</sup>	CM <sub>H</sub>  ,  CM <sub>L</sub>	20	30		kV/μs	V <sub>cm</sub> = 300 V
Channel-to-Channel Skew	t <sub>CSK</sub>		3	5	ns	C <sub>L</sub> = 15 pF
SYNC Timing						
SYNC Time Until Data Valid	t <sub>DVAL</sub>			9	μs	
Internal Clock Off Time <sup>(11)</sup>	t <sub>OFF</sub>			5	ns	
SYNC Pulse Width	t <sub>PWS</sub>	10			μs	
Internal Clock Pulse Width	t <sub>PWI</sub>	3.5		5	ns	
Dynamic Power Consumption <sup>(6)</sup>			200	340	μA/MHz	per channel
<b>Magnetic Field Immunity<sup>(8)</sup> (V<sub>DD2</sub>= 5V, 3V&lt;V<sub>DD1</sub>&lt;5.5V)</b>						
Power Frequency Magnetic Immunity	H <sub>PF</sub>	2800	3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H <sub>PM</sub>	4000	4500		A/m	t <sub>p</sub> = 8 μs
Damped Oscillatory Magnetic Field	H <sub>OSC</sub>	4000	4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier <sup>(9)</sup>	K <sub>X</sub>		2.5			

**Notes (apply to both 3.3 V and 5 V specifications):**

---

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as  $|t_{\text{PHL}} - t_{\text{PLH}}|$ . %PWD is equal to PWD divided by pulse width.
3.  $t_{\text{PSK}}$  is the magnitude of the worst-case difference in  $t_{\text{PHL}}$  and/or  $t_{\text{PLH}}$  between devices at 25°C.
4.  $\text{CM}_\text{H}$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_o > 0.8 V_{\text{DD2}}$ .  $\text{CM}_\text{L}$  is the maximum common mode input voltage that can be sustained while maintaining  $V_o < 0.8 \text{ V}$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins on each side of the package are shorted.
6. Dynamic power consumption is calculated per channel and is supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 9.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 9).
10. If internal clock is used, devices will respond to DC states on inputs within a maximum of 9  $\mu\text{s}$ . Outputs may oscillate if SYNC input slew rate is less than 1 V/ms.
11.  $t_{\text{off}}$  is the maximum time for the internal clock to shut down.

## Application Information

### Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

### Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

Additionally, on the IL510 and IL515, the internal clock can be disabled for even better EMC performance.

These isolators are fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. NVE has completed compliance tests in the categories below:

#### EN50081-1

Residential, Commercial & Light Industrial  
Methods EN55022, EN55014

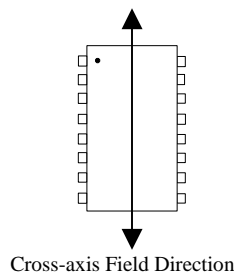
#### EN50082-2: Industrial Environment

Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

#### ENV50204

Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



### Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. A magnetic field is created around the GMR Wheatstone bridge by detecting the edge transitions of the input logic signal and converting them to narrow current pulses. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

### Power Supply Decoupling

Both power supplies to these devices should be decoupled with low ESR ceramic capacitors of at least 47 nF. Capacitors must be located as close as possible to the  $V_{DD}$  pins.

### DC Correctness, EMC, and the SYNC Function

NVE digital isolators have the lowest EMC noise signature of any high-speed digital isolator on the market today because of the dc nature of the GMR sensors used. It is perhaps fair to include opto-couplers in that dc category too, but their limited parametric performance, physically large size, and wear-out problems effectively limit side by side comparisons between NVE's isolators and isolators coupled with RF, matched capacitors, or transformers.

The IL500-Series marks a departure from other NVE coupler families with the inclusion of a patented, controllable refresh clock. The clock ensures that outputs will be synchronized to inputs within 9  $\mu$ s of the supply voltage passing the CMOS circuit's 1.5 V  $V_T$  threshold. Alternatively, on certain models the user can supply an external synchronization clock. There are several advantages to this form of control, the most important being that at power up the user no longer needs to design a synchronization circuit or add firmware to ensure the output is at the same logic level as the input. Unlike other technologies, however, the clock is not required for normal operation and can be gated off to reduce the EMC signature of the end product. This has many advantages in noise-critical applications such as hi-fi audio, motor control, and power conversion. It also allows the use of standard Power on Reset (POR) circuits, common in microcontroller applications, as the means of ensuring the output of the device is in the same state as the input a short time after power up. Figure 1 shows a practical Power on Reset circuit. Decoupling capacitors are omitted for clarity.

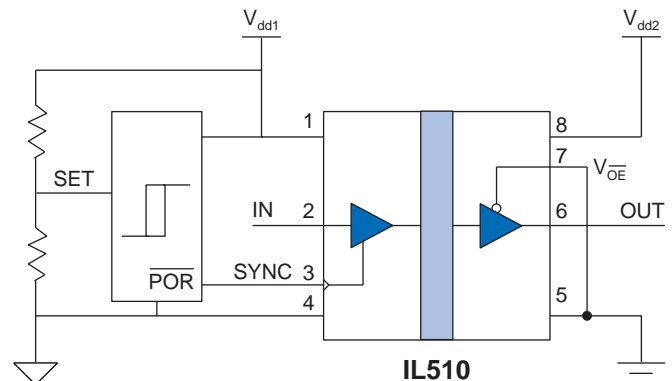


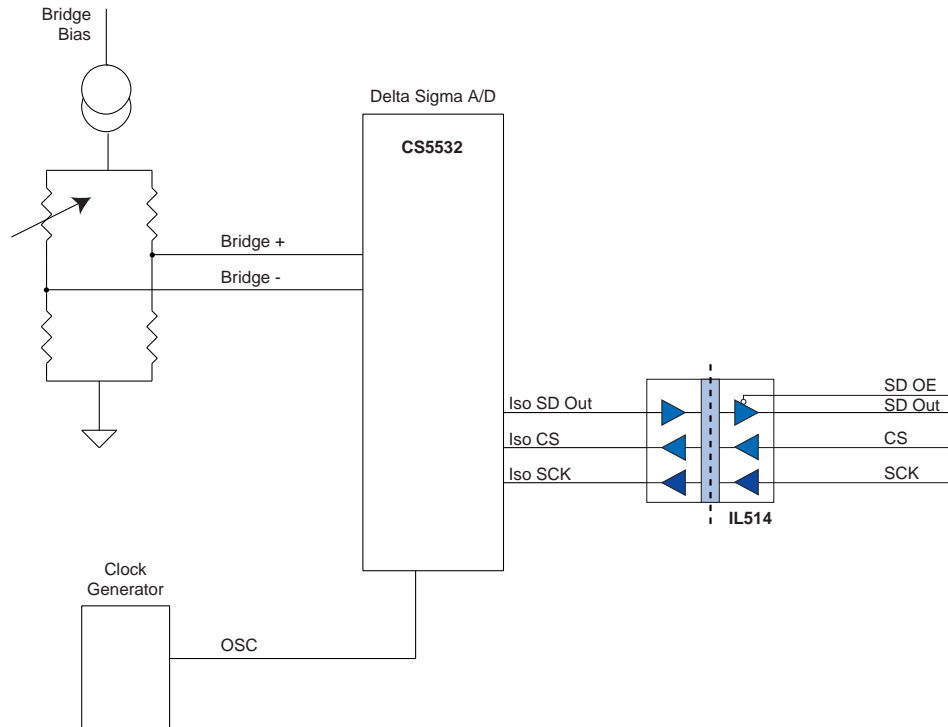
Fig. 1. Typical Power On Reset Circuit for IL510

If multiple devices are used on a board and the designer wants to use the refresh clock in continuous mode, the external clock signal can be provided to each IL5xx Isolator, without the beat-frequency noise problems inherent with competing isolator technologies.

The IL510 and IL515 have the SYNC function available to the user. The IL511, IL514, and IL516 are available in continuous clocking mode only (the user cannot turn off the refresh clock on those devices).

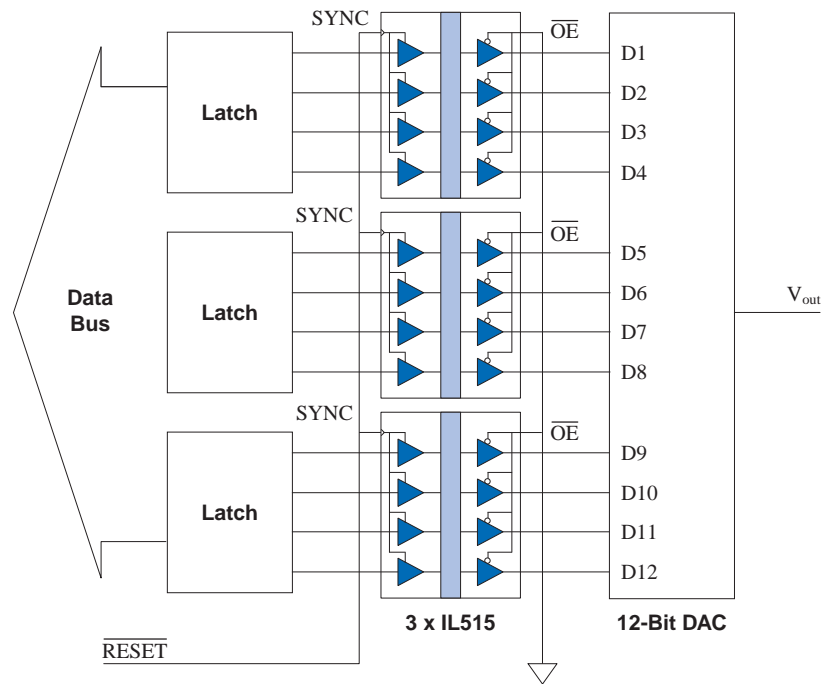
## Illustrative Applications

### Isolated A/D Converter



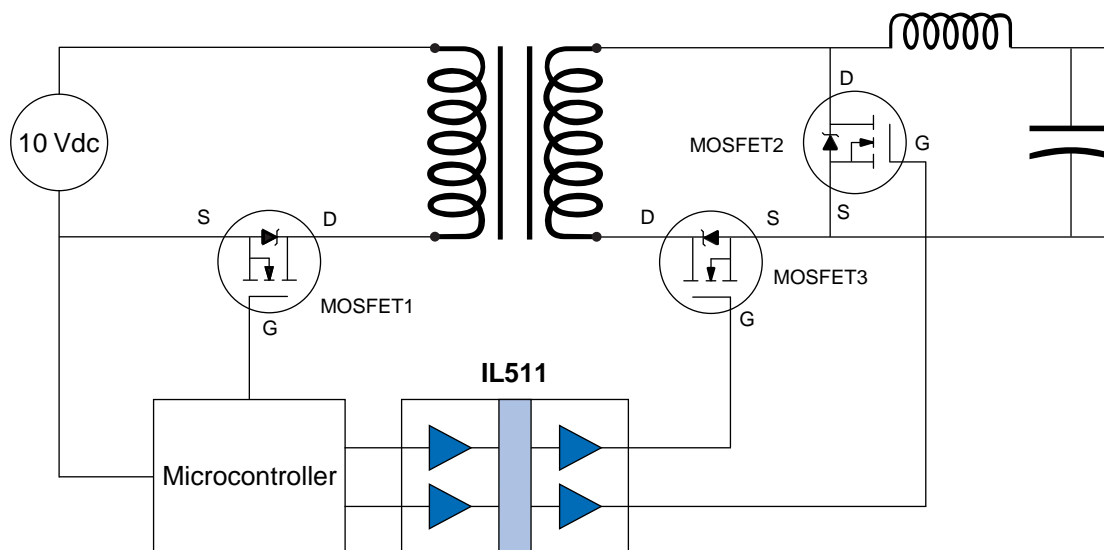
A delta-sigma A-D converter interfaced with the three-channel IL514. Multiple channels can easily be combined using the IL514's output enable function.

**12-Bit D/A Converter Isolation**



The IL515 four-channel isolator is ideally suited for parallel bus isolation. The circuit above uses three IL515s to isolate a 12-bit DAC. The unique SYNC function allows the internal clock to be shut off, eliminating the small amount of noise associated with this clock. A reset pulse is applied at power-on to ensure correct data on the isolator outputs. After the reset pulse goes high, data transfer from input to output is initiated by the leading edge of each changing data bit.

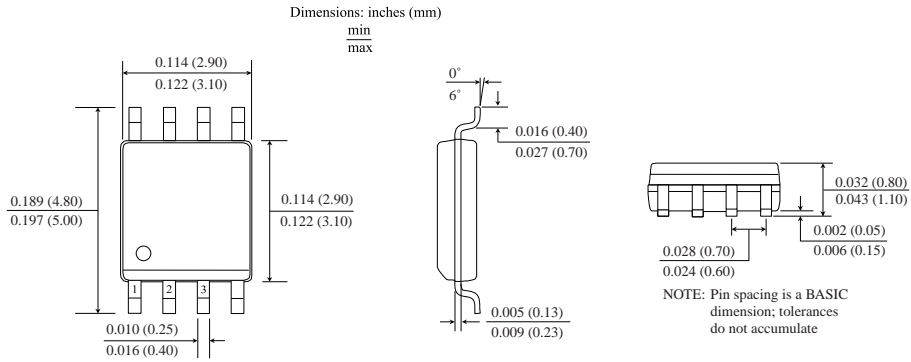
**Intelligent DC-DC Converter With Synchronous Rectification**



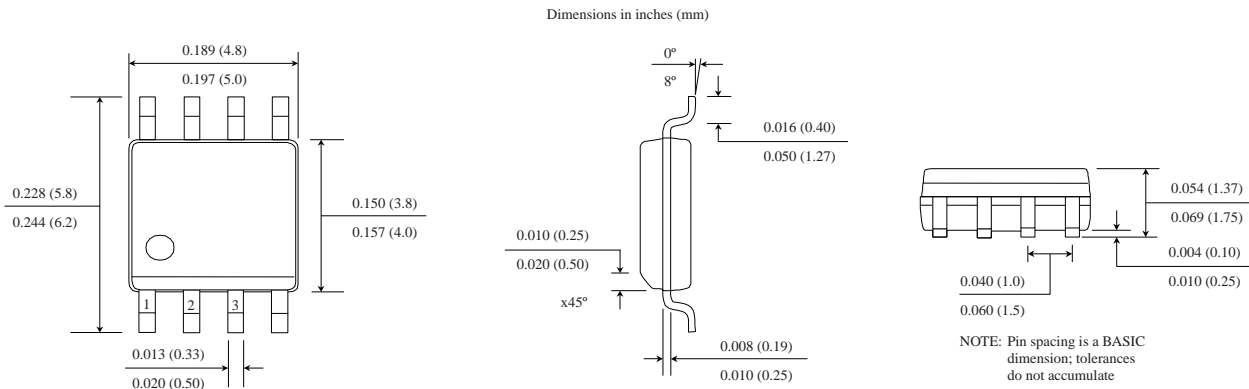
A typical primary-side controller uses the IL511 to drive the synchronous rectification signals from primary side to secondary side. IL511 pulse-width distortion of 10 ns minimizes MOSFET dead time and maximizes efficiency. The ultra-small MSOP package minimizes board area.

## Package Drawings, Dimensions, and Specifications

### 8-pin MSOP



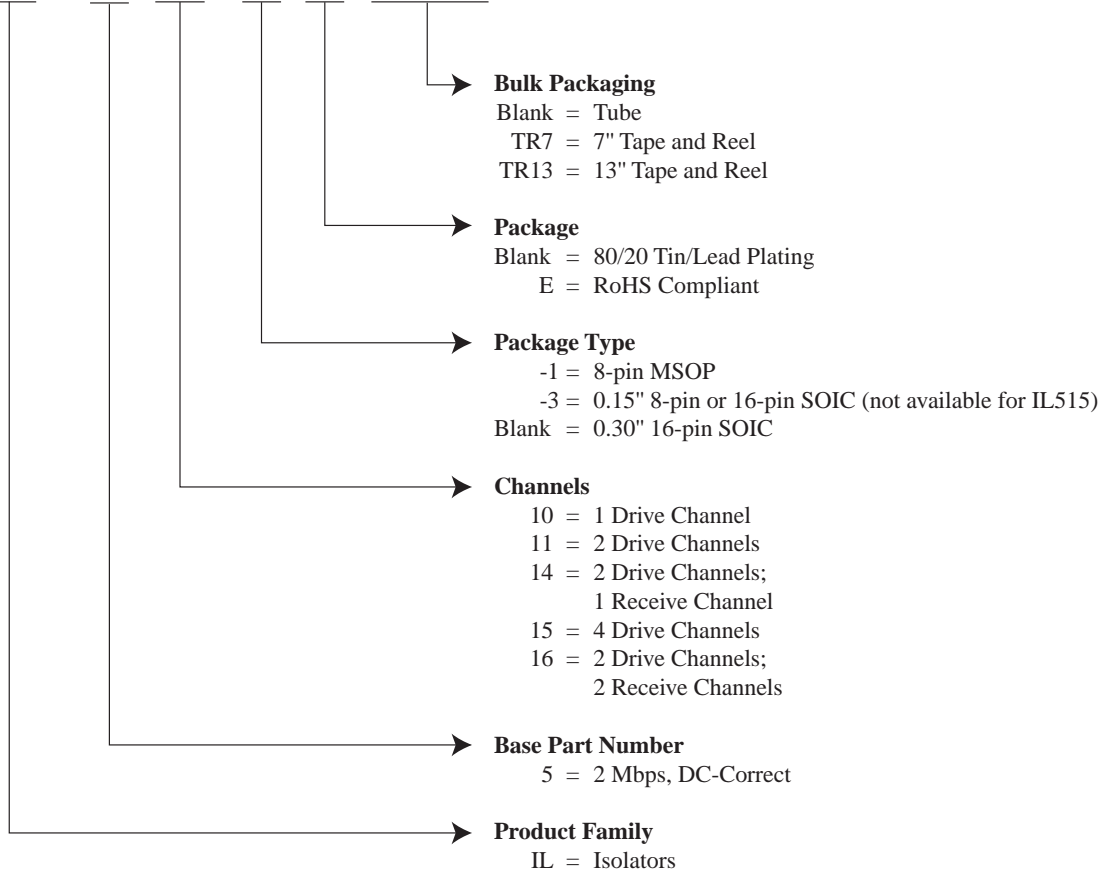
### 8-pin SOIC Package





**Ordering Information**

**IL 5 16 - 3 E TR13**



**ISB-DS-001-IL500-F**  
**September 2010**

**Changes:**

- Changed pin spacing specification on MSOP drawing.

**ISB-DS-001-IL500-E**

**Changes:**

- Added EMC details.

**ISB-DS-001-IL500-D**

**Changes:**

- Add Output Enable to IL515.
- IEC 61010-2001 Approval (removed “pending”).
- Added 12-bit DAC illustrative application.

**ISB-DS-001-IL500-C**

**Production release**

**ISB-DS-001-IL500-B**  
**July 2008**

**Initial release**

**ISB-DS-001-IL500-A**  
**June 2008**

**Preliminary release**

## About NVE

An ISO 9001 Certified Company

NVE Corporation is a high technology components manufacturer having the unique capability to combine spintronic Giant Magnetoresistive (GMR) materials with integrated circuits to make high performance electronic components. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometer), Digital Magnetic Field Sensors, Digital Signal Isolators and Isolated Bus Transceivers.

NVE is a leader in GMR research and in 1994 introduced the world's first products using GMR material, a line of GMR magnetic field sensors that can be used for position, magnetic media, wheel speed and current sensing.

NVE is located in Eden Prairie, Minnesota, a suburb of Minneapolis. Please visit our Web site at [www.nve.com](http://www.nve.com) or call (952) 829-9217 for information on products, sales or distribution.

NVE Corporation  
11409 Valley View Road  
Eden Prairie, MN 55344-3617 USA  
Telephone: (952) 829-9217  
Fax: (952) 829-9189  
Internet: [www.nve.com](http://www.nve.com)  
e-mail: [isoinfo@nve.com](mailto:isoinfo@nve.com)

*The information provided by NVE Corporation is believed to be accurate. However, no responsibility is assumed by NVE Corporation for its use, nor for any infringement of patents, nor rights or licenses granted to third parties, which may result from its use. No license is granted by implication, or otherwise, under any patent or patent rights of NVE Corporation. NVE Corporation does not authorize, nor warrant, any NVE Corporation product for use in life support devices or systems or other critical applications without the express written approval of the President of NVE Corporation.*

***Specifications shown are subject to change without notice.***

ISB-DS-001-IL500-F  
September 2010