TFT-Display Datenblatt

Modell FG020410DNSWBG0Z

Kurzdaten

Hersteller	Data Image
Diagonale	2,4” / 6,1 cm
Format	wide
Auflösung	480 x 234
Backlight	LED / >125 cd/m²
Interface	RGB
Touchscreen	nein
Temperatur	-20…+70°C (Betrieb)

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DATA IMAGE

Confidential Document

DATA IMAGE CORPORATION

TFT Module Specification

ITEM NO.: FG020410DNSWBG0Z

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Customer Companies	R&D Dept.	Q.C. Dept.	Eng. Dept.	Prod. Dept.
Approved by	Version:	Issued Date:	Sheet Code:	Total Pages:
	C	15/JUN/11'		27

2. RECORD OF REVISION

Rev	Date	Item	Page	Comment
A	29/MAY/06'			New Release
B	1/DEC/06'	15	28	Add Stiffener (PET) on FPC.
C	15/JUN/11'	12 14	26 29	1.Modify: LCM PRODUCT LABEL DEFINE· 2.Modify:OUTLINE DRAWING from Rev.B to C

3. Application

This technical specification applies to 2.4” color TFT-LCD panel.
This panel is designed for camcorder, digital camera ,printer and other electronic products which require high quality flat color displays.

4. Features

- Support 8-bit data (RGB) or CCIR656/CCIR601 8 bit format.
- Support the SPI commands setting, the operation parameters setting internally.
- Support Stand-by mode.
- Support PWM LED power driving .
- Right and left shift capability.
- Up and down scan capability.
- Our components and processes are compliant to RoHS standard

5. GENERAL Specifications

Parameter		Specifications	Unit
Screen Size		2.4 (diagonal)	inch
Surface Treatment		Anti-Glare	
Display Format		480 x 234	dots
Active Area		48 (W) x 35.685 (H)	mm
Dot Pitch		0.1(W) x 0.1525 (H)	mm
Pixel Configuration		R.G.B Delta	
Outline Dimension		55.2 (W) x 47.55 (H) x 2.81(T)	mm
Weight		12	g
View Angle direction		6 o’clock	
Temperature Range	Operation	-20~70	℃
	Storage	-30~80	℃

6. Absolute Maximum Ratings:

(GND=PGND=0V)

Parameter	Symbol	MIN.	MAX.	Unit
Power supply voltage (1)	VCC	-0.3	+7.0	V
Power supply voltage (2)	AVDD	-0.3	+7.0	V
Power supply voltage (3)	PVDD	-0.3	+7.0	V
Input voltage	Vin	-0.3	VCC+0.3	V

Note:
All of the voltages listed above are with respective to VSS=0V.
Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

7. Electrical Characteristics

a. Typical operating conditions

(GND=PGND=0V) Ta=25℃

Parameter		Symbol	MIN.	TYP	MAX.	Unit	Remark
Power voltage		VCC	2.7	3.3	3.6	V	
		PVDD,AVDD	3.0	3.3	3.6	V	
		VCOM AC	5.25	5.75	6.25	V	
		VCOM DC	0.7	0.9	1.1		
Input Signal voltage	H Level	VIH	0.7*VCC		VCC	V	
	L Level	VIL	GND		0.3*VCC	V	
Analog stand by current		Ist	-	--	10	μA	PVDD;STB="O" all factions are shut down

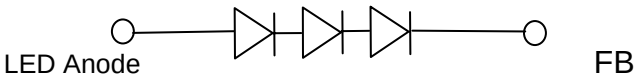
b. Current consumption

(GND=PGND=0V) Ta=25℃

Parameter	Symbol	Condition	MIN.	TYP	MAX.	Unit
	I_{VCC}	Vcc=3.3V		1.5	3.5	mA
	I_{PVDD}	PVDD=3.3V		13.5	60	mA
	I_{AVDD}	AVDD=3.3V		1.2	3.5	mA

C. Backlight Driving for Power Consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_L	--	9.45	11.7	V	I_L=20 mA Ta= 25 ℃
LED current	I_L	--	20	--	mA	Ta= 25 ℃



7.1 AC Characteristics

a.Timing conditions

Parameter	Symbol	MIN.	TYP	MAX.	Unit
Delay between Hsync and DCLK	Thc			1	DCLK
Hysnc width	Twh	1	32		DCLK
Hysnc period	Th	60	63.5	67	μs
Vsync setup time	Tvst	12			ns
Vsync hold time	Tvhd	12			ns
Hsync setup time	Thst	12			ns
Hsync hold time	Thhd	12			ns
Data set-up time	Tdsu	12			ns
Data hold time	Tdhd	12	-		ns
DE set-up time	Tesu	12	-		ns
Vsync width	Twv	2	4	6	Th
Vsync period NTSC	Tv		262.5		Th
Vsync period PAL	Tv	-	312.5	--	Th
Hsync to Vsync time for ODD field	THV O	-4		+4	DCLK
Hsync to Vsync time for EVEN field	THV E	-	0.5		Th
S/D output stable time	Tst			30	μs
G/D output stable time	Tgst		1		μs

b. Operating mode dependent AC characteristic

Serial RGB Mode, SEL [2…0]=[000, 001]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk		9.7		Mhz
DCLK period	Tcph		103		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso		56		DCLK
Delay from Hsync to Gate output	Thgo		45		DCLK
Delay from Hsync to Gate output off	Thgz		19		DCLK
Delay from Hsync to FRP	Thf		56		DCLK
Delay from Hsync to 1st data input **(for SYNC mode)**	Ths	83	99	114	DCLK

c. Operating mode dependent AC characteristic

YUV Mode, SEL [2…0]=[011~110]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk		24.54/27		Mhz
DCLK period	Tcph		40.7/37		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from Hsync to Source output	Thso		143		DCLK
Delay from Hsync to Gate output	Thgo		113		DCLK
Delay from Hsync to Gate output off	Thgz		48		DCLK
Delay from Hsync to FRP	Thf		143		DCLK
Delay from Hsync to 1,st data input (for TS601=0)	Ths	233	249	264	DCLK

d. Operating mode dependent AC characteristic

CCIR656 Mode (720 x 480 pixel), SEL [2…0]=[111]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk	-	27	-	Mhz
DCLK period	Tcph		37		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso		171		DCLK
Delay from CCIR_H to Gate output	Thgo		141		DCLK
Delay from CCIR_H to Gate output off	Thgz		76		DCLK
Delay from CCIR_H to FRP	Thf		171		DCLK

e. Operating mode dependent AC characteristic

CCIR656 Mode (640 x 480 pixel), SEL [2…0]=[010]

Parameter	Symbol	MIN.	TYP	MAX.	Unit
DCLK frequency	Fclk	-	24.54	-	Mhz
DCLK period	Tcph		40.7		ns
DCLK duty cycle	Tcw	40	50	60	%Tcph
Delay from CCIR_H to Source output	Thso		171		DCLK
Delay from CCIR_H to Gate output	Thgo		141		DCLK
Delay from CCIR_H to Gate output off	Thgz		76		DCLK
Delay from CCIR_H to FRP	Thf		171		DCLK

7.2 Waveform:

7.2.1 Timing format: Serial communication timing:

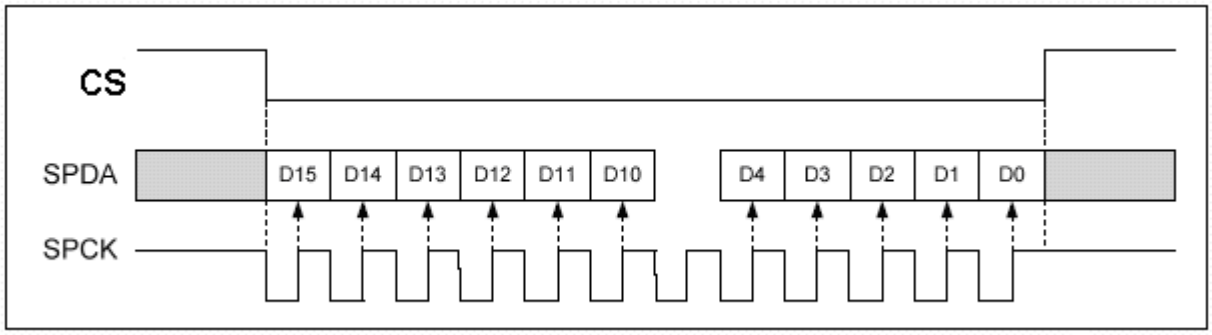
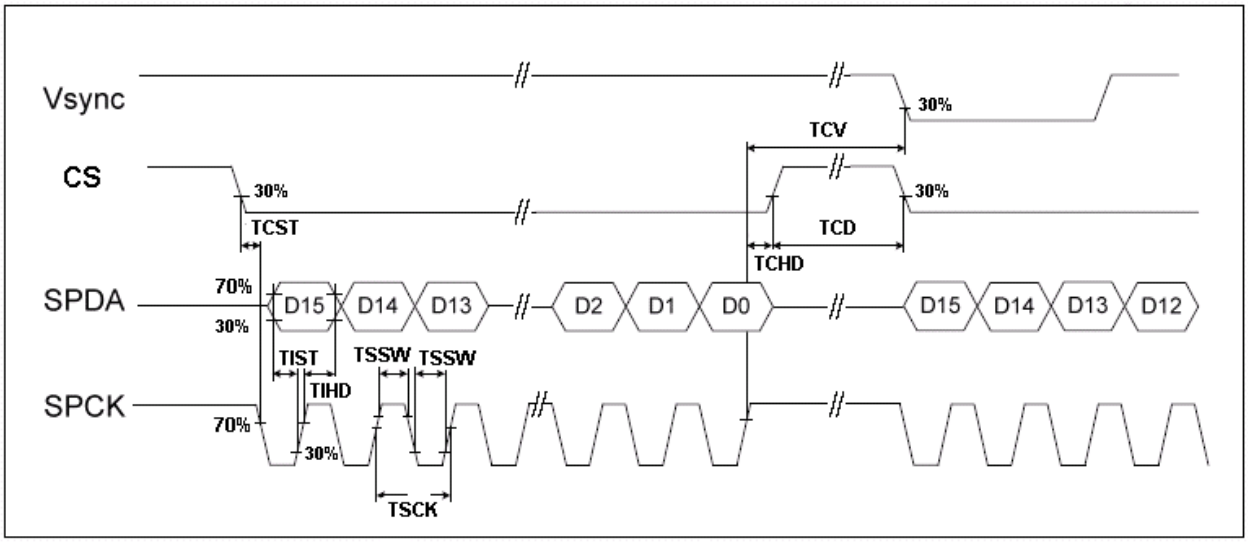


Figure 7.2 SPI Timing Diagram



Note: All the SPI register settings will active at the falling edge of the VSYNC except GRB_STB and SEL[2:0] bits_

Figure 7. 2.1 SPI Timing Diagram V.S. Vsync

7.2.2 Serial communication

Parameter	Symbol	MIN.	TYP	MAX.	Unit
Serial clock period	Tsck	320	-	-	ns
Serial clock duty cycle	Tscw	40	50	60	%
Serial clock width	Tssw	120	-	-	ns
Serial data setup time	Tist	120	-	-	ns
Serial data hold time	Tihd	120	-	-	ns
SPENB setup time	Tcst	120	-	-	ns
SPENB data hold time	Tchd	120	-	-	ns
Chip select distinguish	Tcd	1	-	-	µs
Delay between SPCK and Vsync	Tcv	1	-	-	µs

Note: The first valid data line on panel is G1=Tstv+1=14(Active area is 240 channels).

7.3 Clock and Data Input Timing Diagram

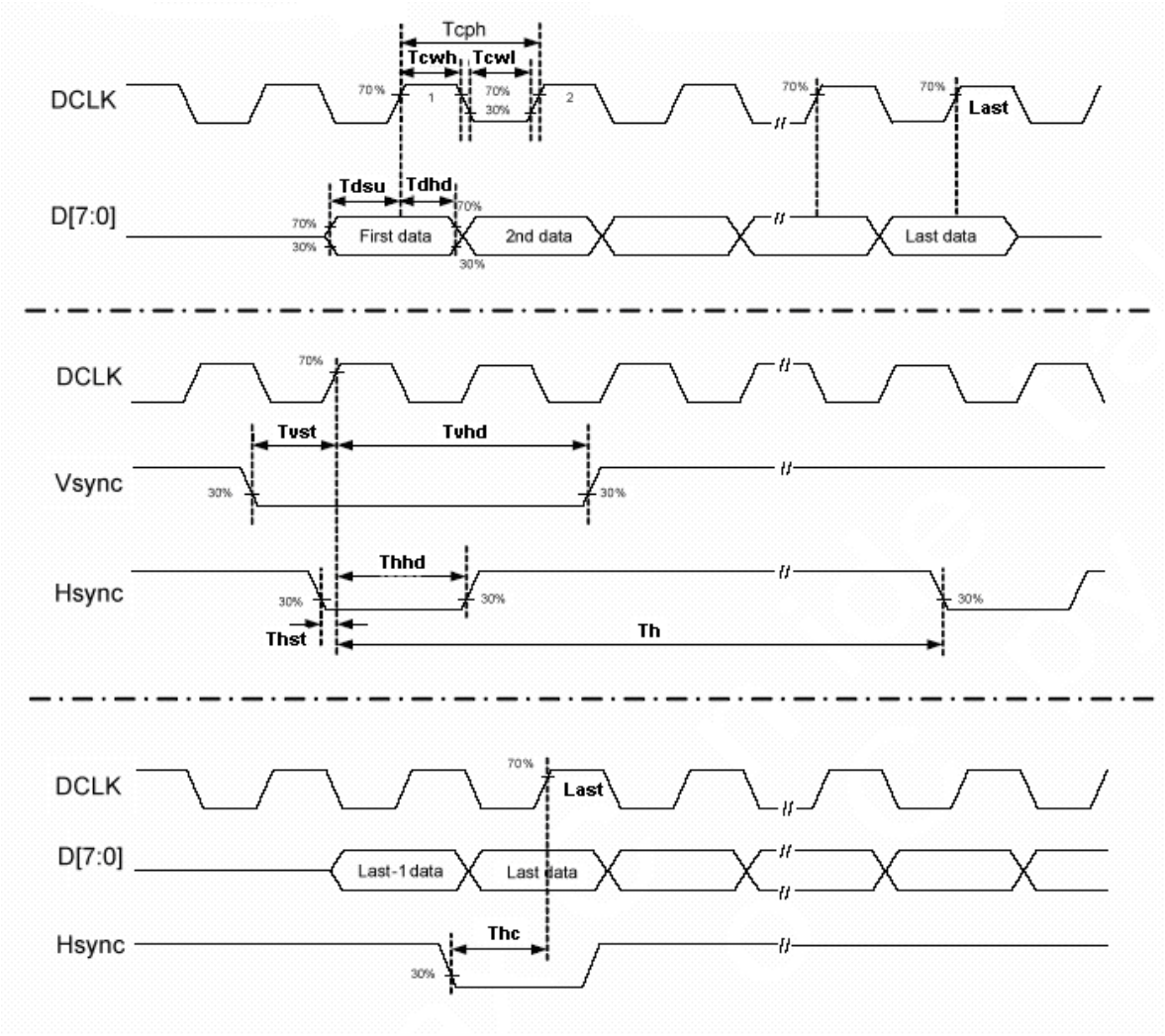


Figure7.3 Clock and Data Input Timing Diagram

7.4 Source Driver Output Timing Chart (IC internal timing, for user reference)

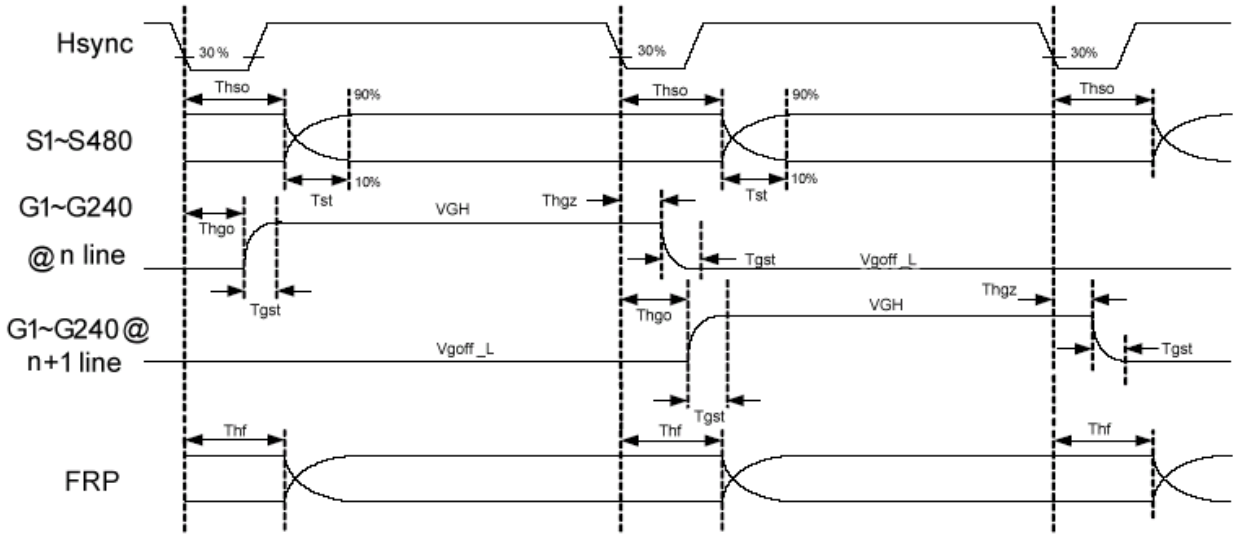


Figure 7.4 Source Driver and VCOM (FRP) Output Timing Chart

7.5 Input Data Format Timing

7.5.1 Serial RGB Data Format

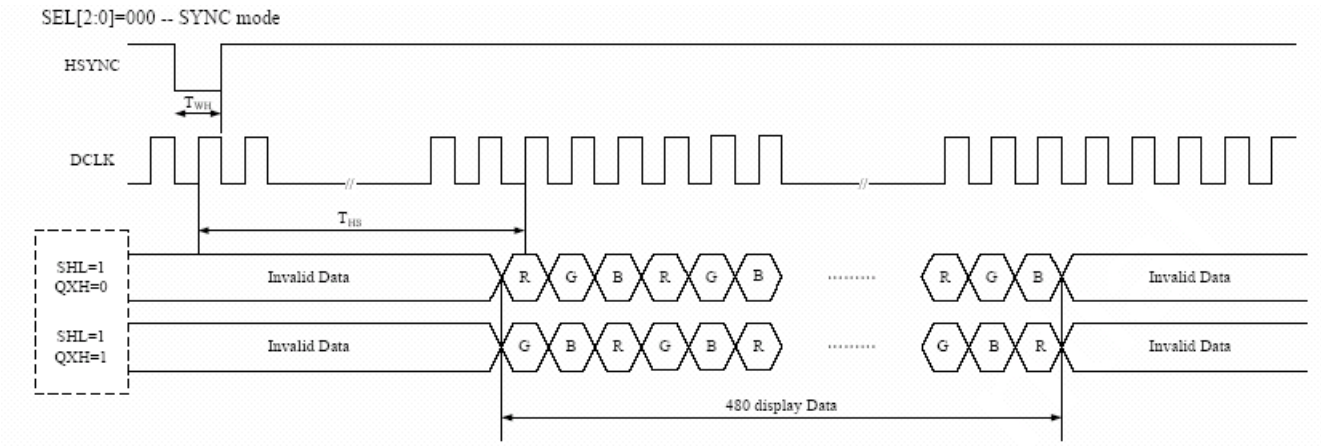


Figure 7.5.1 Serial RGB Data Format

7.5.2 YUV mode Data Format

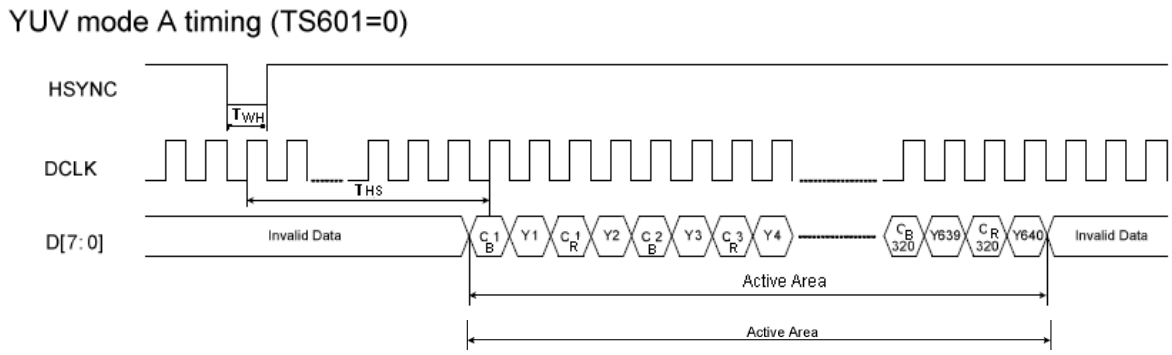


Figure 7.5.2 YUV Mode Data Format

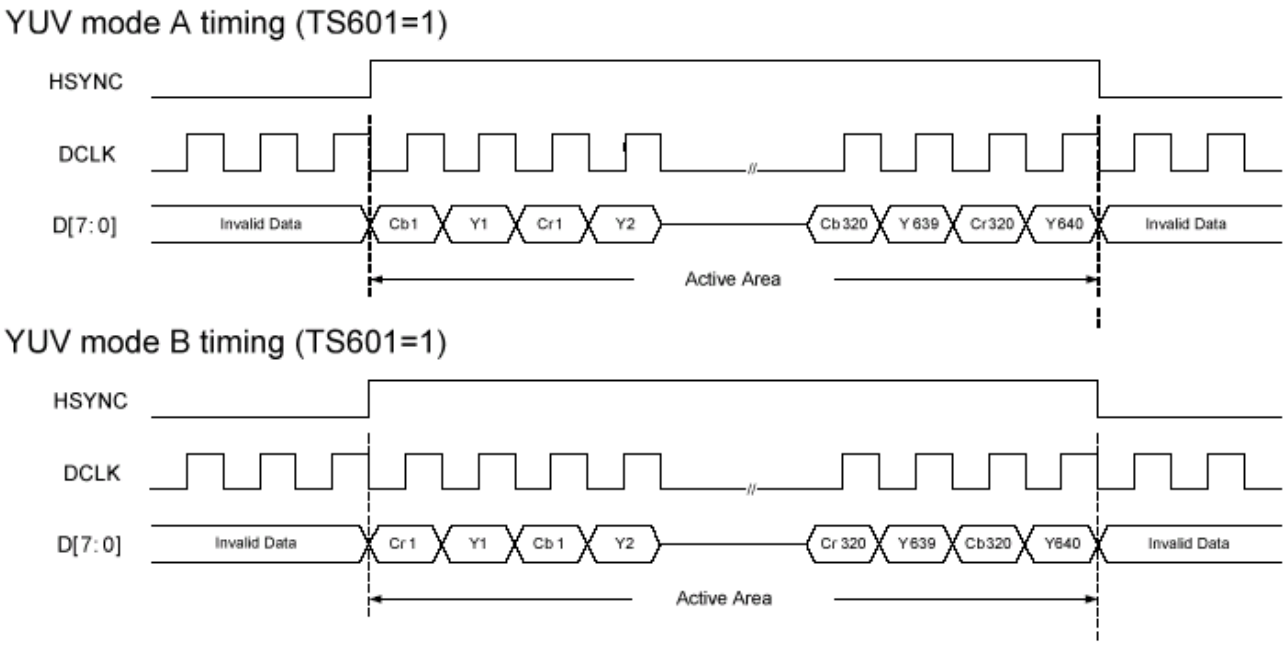


Figure 7.5.2.1 YUV Mode Data Format, TS601=1, HSDPOL=0

Input format	DCLK Freq (MHz)	Display Data	Active Area (DCLK)
YUV mode	24.54	640	1280
	27	720	1440

7.5.3 CCIR656 Data Format

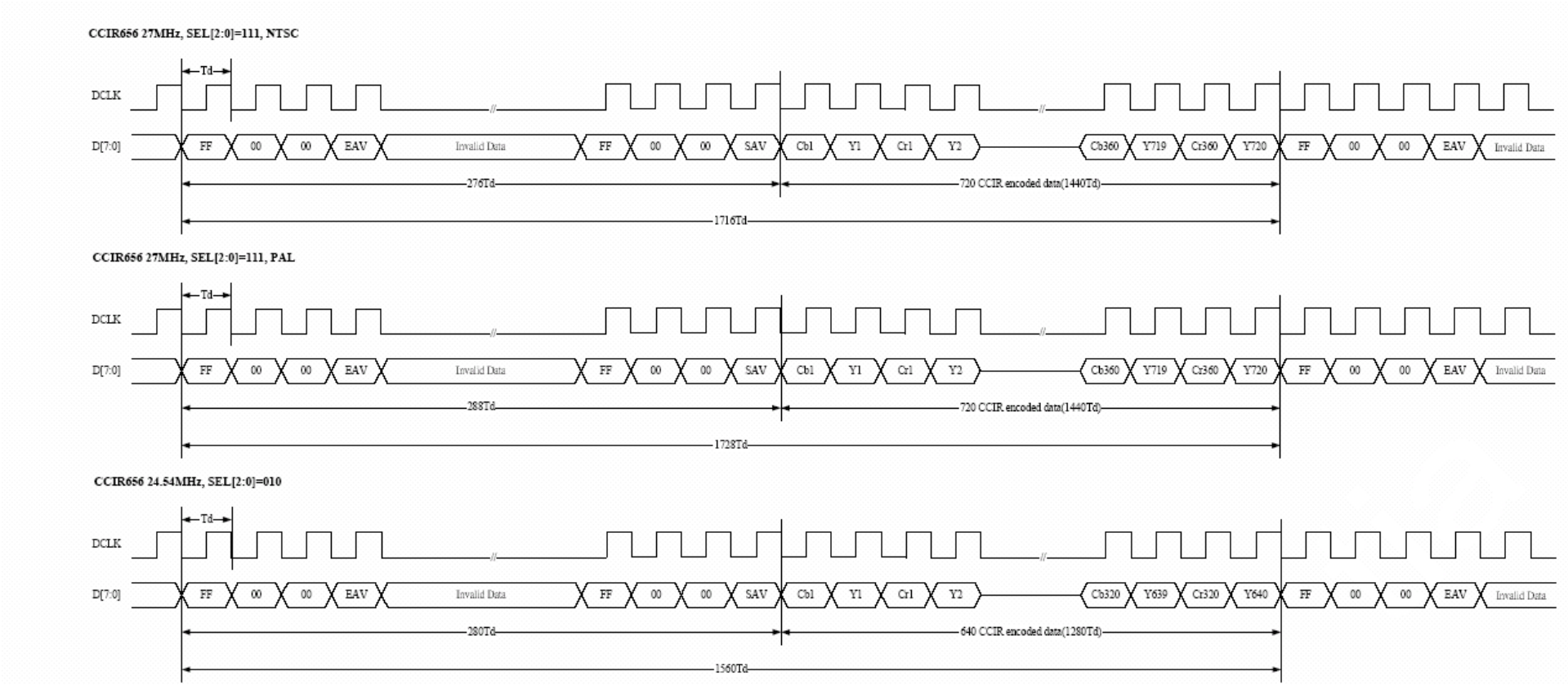


Figure7.5.3 CCIR656 Data Format

7.6 Power ON/OFF sequence

Specially take care that the large current may cause a permanent damage to the IC when voltage is applied to the charge pump power supply in the condition that the logic power supply is floating.
Please refer to the following timing and command setting, concerning the power supply ON and the power supply OFF.

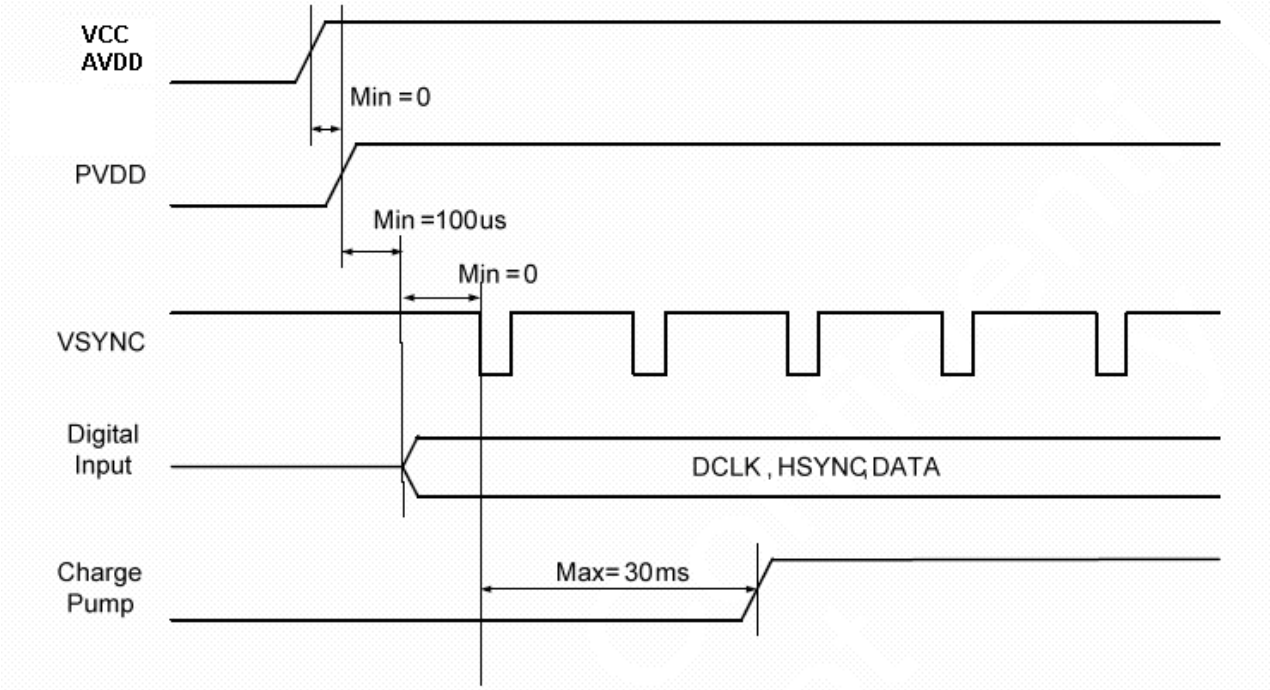


Figure7.6 Power on sequence timing diagram

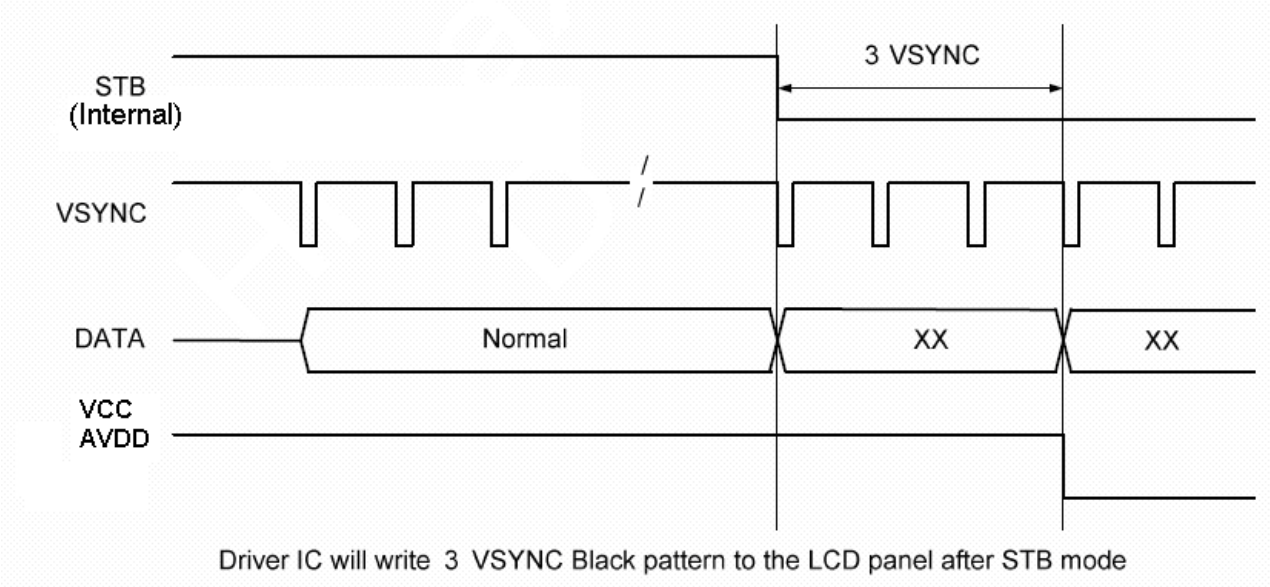
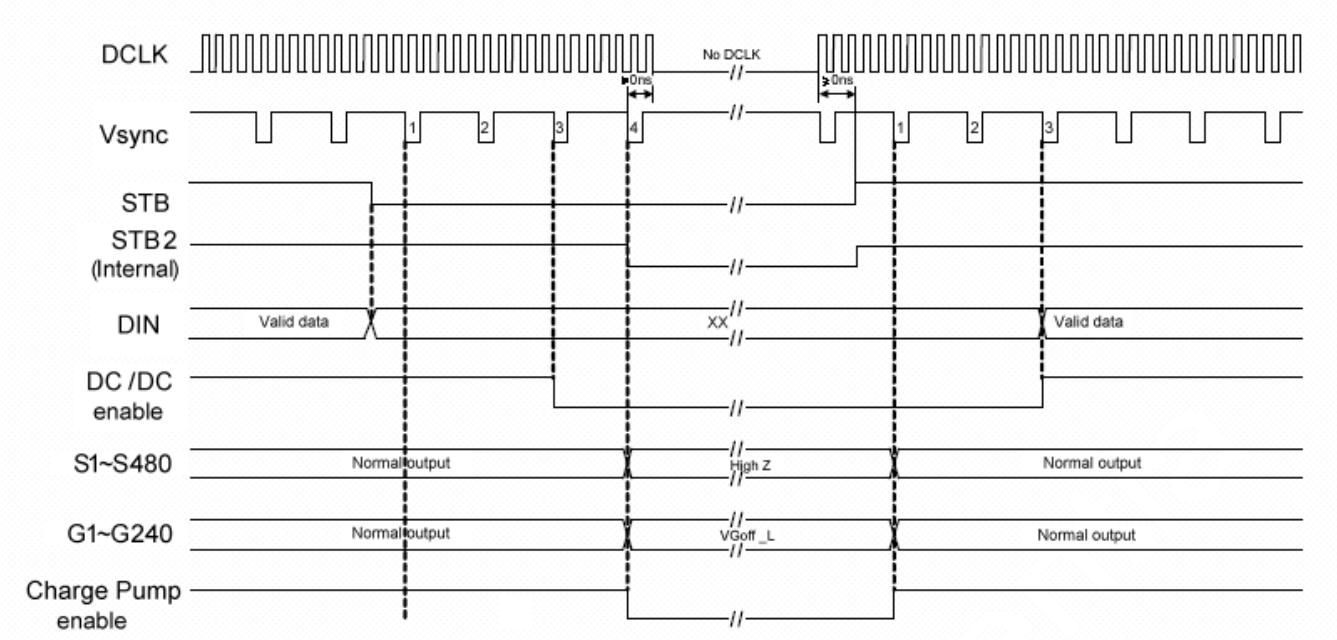


Figure 7.6.1 Power off sequence timing diagram



During No CLK, Hsync and Vsync can be stopped. But in all other cases Hsync and Vsync must be active

Figure 7.6.2 Enter and exit stand-by mode timing diagram

8. Register Description

Register	Function Description
R00	System Setting Register
R01	Timing Control Setting Register
R02	Driver Setting Register
R03	Data format Setting Register
R04	Source Delay Setting Register
R05	Vertical Delay Setting Register
R06	Voltage Level Setting Register
R07	Internal Setting Register

Table 8.1 Function Description

8.1 Function Control Register

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	Register Address			Data												
R00	0	0	0	0					*Reserved*	*Reserved*	*Reserved*	*Reserved*	GRB	STB	SHDB	SHCB
R01	0	0	1	0					*Reserved*	*Reserved*	SWD2	SWD1	SWD0	DITB	OEA1	OEA0
R02	0	1	0	0					*Reserved*	*0*	INSET1	INSET0	FPOL	none	UD	SHL
R03	0	1	1	0					TS601	HSDPOL	VSDPOL	PALM	PAL	SEL2	SEL1	SEL0
R04	1	0	0	0					*Reserved*	*Reserved*	*Reserved*	DDL4	DDL3	DDL 2	DDL1	DDL0
R05	1	0	1	0					*Reserved*	*Reserved*	*Reserved*	*Reserved*	HDL3	HDL2	HDL1	HDL0
R06	1	1	0	0					0	0	0	0	0	VSCL2	VSCL1	VSCL0
R07	1	1	1	0					*Reserved*	0	0	0	0	0	1	1

Note 1：D12 must be low。
Note 2：All the SPI register settings will active at the falling edge of the VSYNC except GRB、STB and SEL[2:0] bits。

8.2 System Setting Register (R00h), default = 0Eh

	D15	D14	D13	D12	D11	D10	D9	D8	*D7*	*D6*	*D5*	*D4*	D3	D2	D1	D0
R00	0	0	0	0					*Reserved*	*Reserved*	*Reserved*	*Reserved*	GRB	STB	SHDB	SHCB
	0	0	0	0					*0*	*0*	*0*	*0*	1	1	0	1

GRB	Global Reset
L	The Controller is resets, the Charge Pump and DC/DC is off.
H	Normal operation; Default setting.

STB	Stand By Mode
L	TCON, SD, Charge Pump and DC-DC are off. All outputs are High-Z.
H	Normal operation; Default setting.

SHDB	DC-DC converter shutdown signal
L	The DC-DC is off. Default Setting. (DRV output pin is “LOW”
H	The DC-DC is on. (DRV output pin is working)

Note: The function disable, the DRV output be VSS.

SHCB	Charge Pump shutdown signal
L	The Charge Pump for VGH VGL VCAC are off
H	The Charge Pump is on; Default setting.

8.3 Color dot arrangement Setting Register (R01h), default = 01h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R01	0	0	1	0					Reserved	Reserved	SWD2	SWD1	SWD0	DITB	OEA1	OEA0
	0	0	1	0					0	0	0	0	0	0	0	1

SWD[2:0] Control and switch the relationship between the R, G, B and outputs. (Default = 000 for this color dot fixed panel, don’t need to change it)

DITB	Dithering setting
L	Dithering on 8-bit resolution. Default Setting.
H	Dithering off. 6-bit resolution (the last 2-bits truncated).

OEA1	OEA0	Odd/ Even field Advanced Function, Default value=01.
0	0	Display Start @ HDL delay for Odd field and @***HDL-1***for Even field.
0	1	Display Start @ HDL delay for Odd field and @ ***HDL***for Even field.
1	0	Display Start @ HDL delay for Odd field and @ ***HDL+1*** for Even field.
1	1	Display Start @ HDL delay for Odd field and @ ***HDL***for Even field.

8.4 Driver Setting Register (R02h), default = 03h

	D15	D14	D13	D12	D11	D10	D9	D8	*D7*	*D6*	*D5*	*D4*	**D3**	**D2**	**D1**	**D0**
R02	0	1	0	0					*Reserved*	*Reserved*	INSET 1	INSET0	FPOL	X	UD	SHL
	0	1	0	0					0	0	0	0	0	0	1	1

INSET[1:0]	Input data sequence control
LL,LH	Input data sequence = color filter sequence. Default setting.
HL	Input data sequence = RGB 、GBR(SHL=1、UD=1).
HH	Input data sequence = RGB 、BRG(SHL=1、UD=1).

FPOL	Control the inversion of FRP depending on the polarity of the Gamma Correction
L	FRP in phase with the polarity of the gamma correction.
H	FRP inverted with respect to the polarity of the gamma correction. Default setting.

UD	UP/DOWN Scan Control of Gate Driver
L	Scan up. G240->G239->…..->G2->G1.
H	Scan down. G1->G2->…..->G239->G240. Default Setting.

SHL	Left/Right Selection
L	Shift left. S480->S479->……->S2->S1.
H	Shift right. S1->S2->……->S479->S480. Default Setting.

8.5 Data format Setting Register (R03h), default = 00h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R03	0	1	1	0					TS601	HSDPOL	VSDPOL	PALM	PAL	SEL2	SEL1	SEL0
	0	1	1	0					0	0	0	0	0	0	0	0

TS601	YUV mode (CCIR601) timing selection
L	Timing mode 1. Default setting.
H	Timing mode 2.

HSDPOL	HSYNC polarity control
L	HSYNC negative polarity. Default setting.
H	HSYNC positive polarity.

VSDPOL	VSYNC polarity control
L	VSYNC negative polarity.
H	VSYNC positive polarity.

YUV mode TS601=H→Default value = H, others = L.

PALM	PAL Selection Signal (only available when PAL=H)
L	Input data format is PAL 1/6,8(280 active line). Default Setting.
H	Input data format is PAL 1/6(288 active line).

PAL	NTSC/PAL Selection Signal
L	Input data format is NTSC. Default Setting.
H	Input data format is PAL.

Select Input Data Format, Default Setting=000.

SEL2	SEL1	SEL0	Format	Operating Frequency
0	0	0	Serial-RGB data format (HV mode)	9.7MHz
0	0	1	Serial-RGB data format (DE mode)	9.7MHz
0	1	0	CCIR 656 data format(640RGB)	24.54MHz
0	1	1	YUV mode A data format	24.54MHz
1	0	0	YUV mode A data format	27MHz
1	0	1	YUV mode B data format	24.54MHz
1	1	0	YUV mode B data format	27MHz
1	1	1	CCIR 656 data format(720RGB)	27MHz

8.6 Source Delay Setting Register (R04h), default = 00h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R04	1	0	0	0					*Reserved*	*Reserved*	*Reserved*	DDL4	DDL3	DDL2	DDL 1	DDL 0
	1	0	0	0					0	0	0	0	0	0	0	0

Select the data delay timing, Default Setting=00000.

DDL4	DDL3	DDL2	DDL1	DDL0	Delay	Unit
0	0	0	0	0	0	DCLK Period
0	0	0	0	1	1	
0	0	0	1	0	2	
0	0	0	1	1	3	
0	0	1	0	0	4	
0	0	1	0	1	5	
0	0	1	1	0	6	
0	0	1	1	1	7	
0	1	0	0	0	8	
0	1	0	0	1	9	
0	1	0	1	0	10	
0	1	0	1	1	11	
0	1	1	0	0	12	
0	1	1	0	1	13	
0	1	1	1	0	14	
0	1	1	1	1	15	
1	0	0	0	0	-1	
1	0	0	0	1	-2	
1	0	0	1	0	-3	
1	0	0	1	1	-4	
1	0	1	0	0	-5	
1	0	1	0	1	-6	
1	0	1	1	0	-7	
1	0	1	1	1	-8	
1	1	0	0	0	-9	
1	1	0	0	1	-10	
1	1	0	1	0	-11	
1	1	0	1	1	-12	
1	1	1	0	0	-13	
1	1	1	0	1	-14	
1	1	1	1	0	-15	
1	1	1	1	1	-16	

8.7Vertical Delay Setting Register (R05h), default = 00h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R05	1	0	1	0					*Reserved*	*Reserved*	*Reserved*	*Reserved*	HDL3	HDL2	HDL1	HDL0
	1	0	1	0					0	0	0	0	0	0	0	0

Select the first active line delay timing, Default Setting=0000.

HDL3	HDL2	HDL1	HDL0	Delay	Unit
0	0	0	0	0	HSYNC. Period.
0	0	0	1	1	
0	0	1	0	2	
0	0	1	1	3	
0	1	0	0	4	
0	1	0	1	5	
0	1	1	0	6	
0	1	1	1	7	
1	0	0	0	8	
1	0	0	1	-1	
1	0	1	0	-2	
1	0	1	1	-3	
1	1	0	0	-4	
1	1	0	1	-5	
1	1	1	0	-6	
1	1	1	1	-7	

8.8 Voltage Level Setting Register (R06h), default = 06h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R06	1	1	0	0					X	X	X	X	X	VSCL2	VSCL1	VSCL0
	1	1	0	0					0	0	0	0	0	1	1	0

VCOM amplitude control, default setting=110.

VSCL2	VSCL1	VSCL0	VCAC Level	Unit
0	1	0	4.75	V
0	1	1	5.0	
1	0	0	5.25	
1	0	1	5.5	
1	1	0	5.75	
1	1	1	6.0	
0	0	0	6.25	
0	0	1	6.375	

8.9 Internal Setting Register (R07h), default = 03h

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R07	1	1	1	0					X	X	X	X	X	X	X	X
	1	1	1	0					0	0	0	0	0	0	1	1

(factory use only, don't need to change it).

9. Optical Characteristics

9-1. Specification:

Ta = 25°C

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	ϕ	CR≥10	±45	±50		deg	Note 9-2
	Vertical	θ (to 12 o'clock)		45	50		deg	
		θ (to 6 o'clock)		35	40		deg	
Contrast Ratio		CR		150	--			Note 9-1
Response time	Rise	Tr	θ=0° ϕ=0°		15	30	ms	Note 9-4
	Fall	Tf			35	50	ms	
Uniformity		U			70		%	Note 9-5
Brightness				125	--	--	cd/m^2	Note 9-2

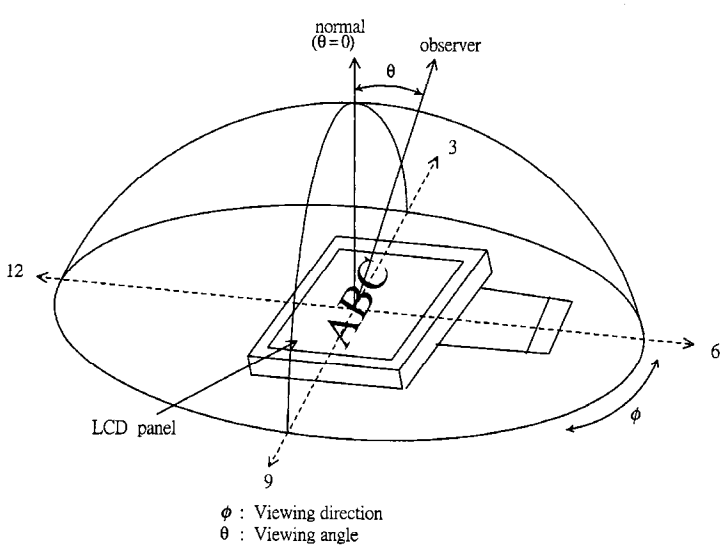
Note 9-1：CR ＝ $\frac{\text{Luminance when LCD is White}}{\text{Luminance when LCD is Black}}$

Contrast Ratio is measured in optimum common electrode voltage.
The test configurations of contrast ratio see section9-2 .

Note 9-2 :1.Topcon BM-7(fast) luminance meter 1.0° field of view is used in the testing (after 2 minutes operation).

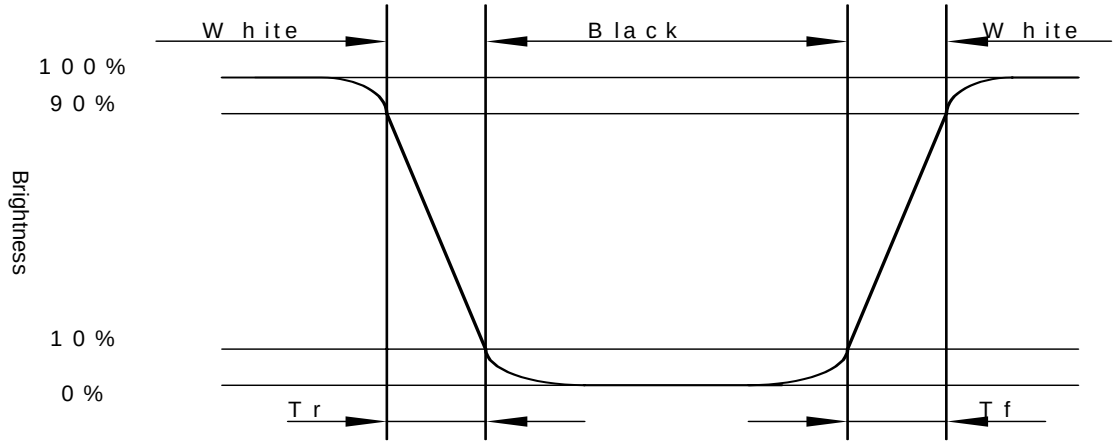
2. LED current =20mA.

Note 9-3 : The definitions of viewing angles diagrams:

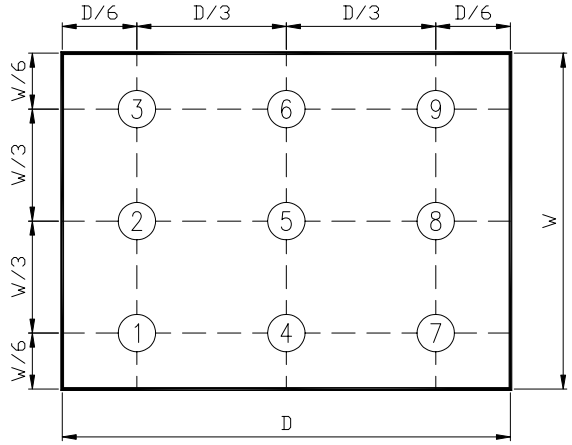


ϕ : Viewing direction
θ : Viewing angle

Note 9-4: The definition of response time:

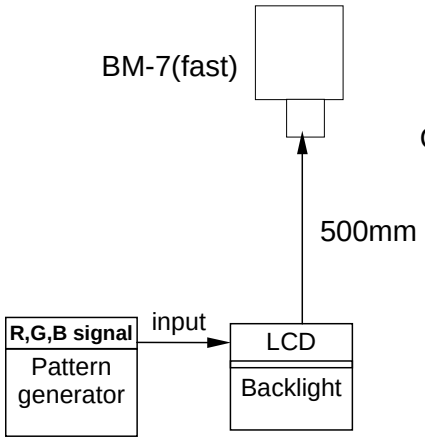


Note 9-5: Definition of Brightness Uniformity (Buni):



$$Buni = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}}$$

9-2. Testing configuration



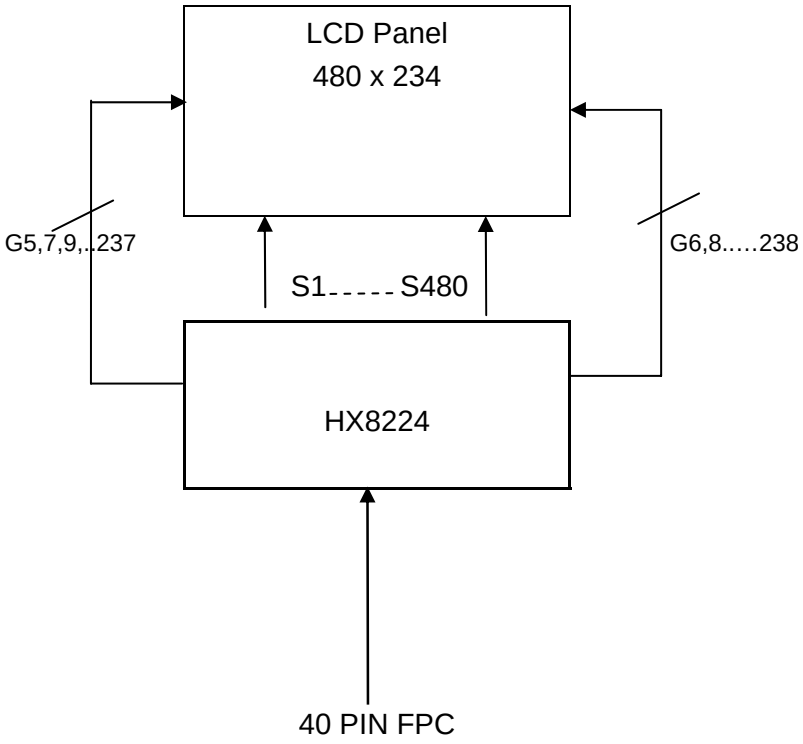
Caution: 1. Environmental illumination≦1 lux
2. Before test CR, Vcom voltage must be adjusted carefully to get the best CR.

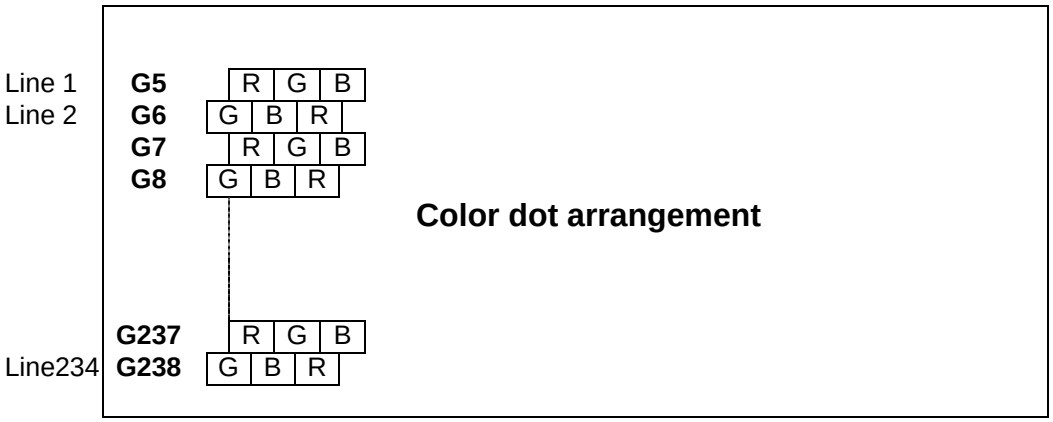
10. Input / Output Terminals

10-1 PIN Connections

Pin no	Symbol	I/O	Description
1	VCOM	I	Common electrode driving voltage
2	NC	--	No Connection
3	Vgoff_L	PO	Negative low power supply for gate driver output: -12.5V
4	C4P	C	Pins to connect capacitance for power circuitry
5	C4M	C	Pins to connect capacitance for power circuitry
6	VGH	PO	Positive power supply for gate driver output: +12.5V
7	FRP	O	Frame polarity output for VCOM
8	VCAC	C	Define the amplitude of the VCOM swing
9	Vint3	P	Intermediate voltage for charge Pump
10	C3P	C	Pins to connect capacitance for power circuitry
11	C3M	C	Pins to connect capacitance for power circuitry
12	Vint2	P	Intermediate voltage for charge Pump
13	C2P	C	Pins to connect capacitance for power circuitry
14	C2M	C	Pins to connect capacitance for power circuitry
15	Vint1	P	Intermediate voltage for charge Pump
16	C1P	C	Pins to connect capacitance for power circuitry
17	C1M	C	Pins to connect capacitance for power circuitry
18	PGND	P	Charge Pump Power GND
19	PVDD	P	Charge Pump Power VDD
20	DRV	PO	Gate signal for the power transistor of the boost converter
21	LED Anode	I	For Led Anode voltage
22	GND	P	Digital GND
23	FB	P	Main boost regulator feedback input
24	AVDD	P	Analog power supply
25	GND	P	Digital GND
26	VCC	P	Digital power supply
27	CS	I	Serial communication chip select
28	SDA	I	Serial communication data input
29	SCL	I	Serial communication clock input
30	HSYNC	I	Horizontal sync input
31	VSYNC	I	Vertical sync input
32	DCLK	I	Clock Input:
33	D7	I	Data input :MSB
34	D6	I	Data input
35	D5	I	Data input
36	D4	I	Data input
37	D3	I	Data input
38	D2	I	Data input
39	D1	I	Data input
40	D0	I	Data input: LSB

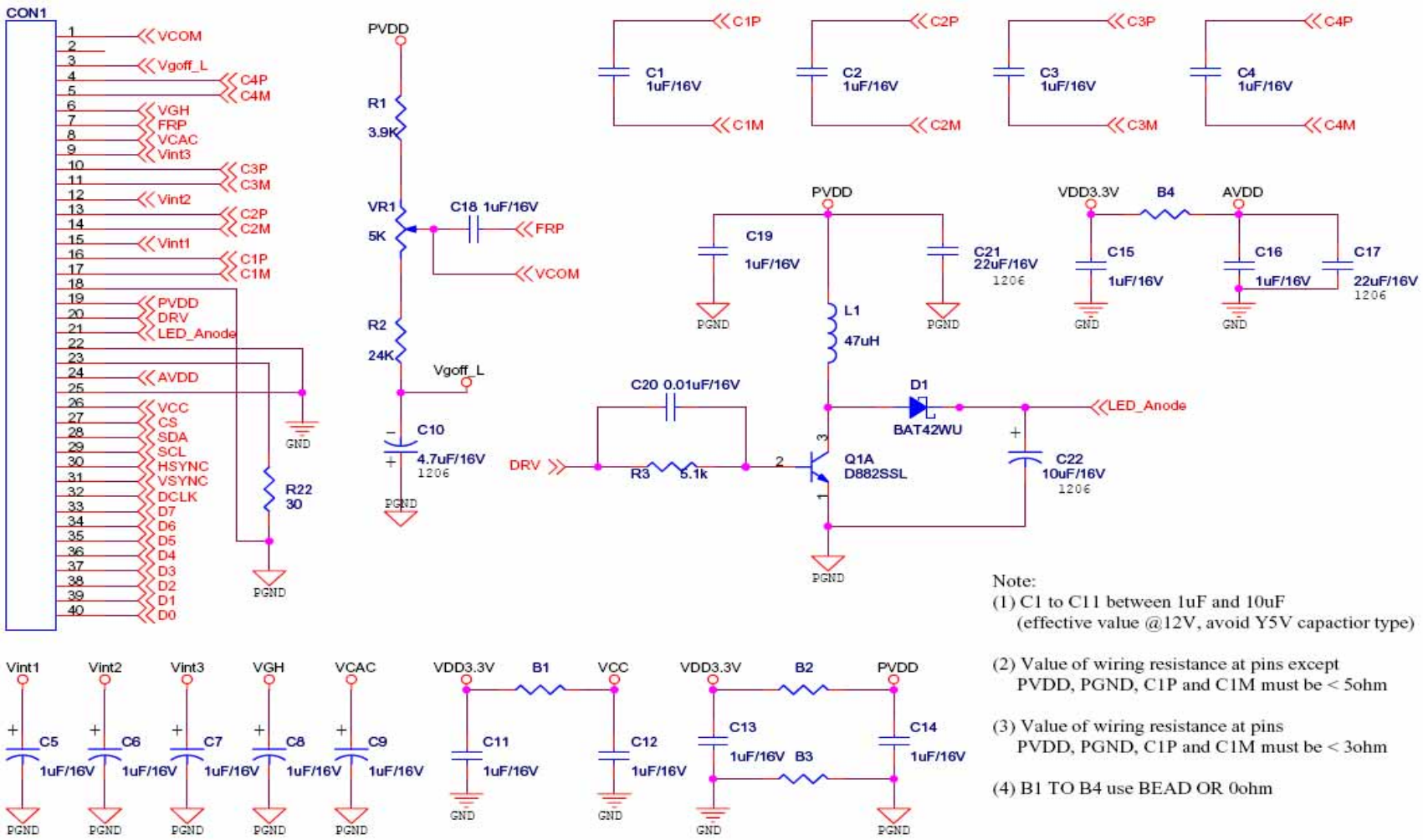
11. Block Diagram





11.1 Application Circuit

11.1.2 With LED Backlight Driving Circuit, FPC, Power connection and LED Backlight Driving Circuit



Note:

(1) C1 to C11 between 1uF and 10uF
(effective value @12V, avoid Y5V capactior type)

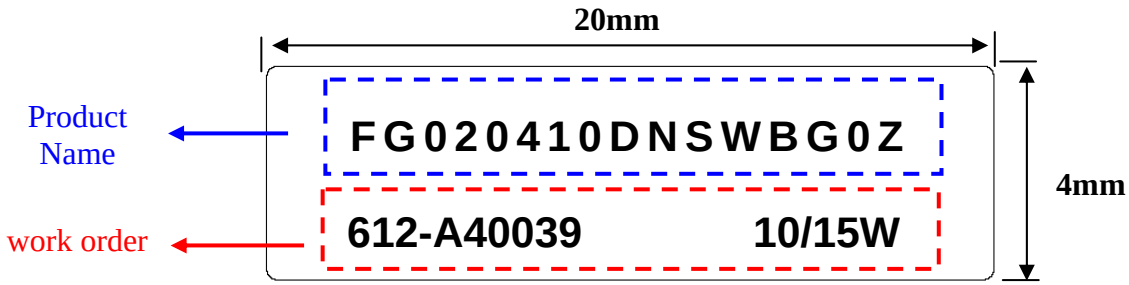
(2) Value of wiring resistance at pins except PVDD, PGND, C1P and C1M must be < 5ohm

(3) Value of wiring resistance at pins PVDD, PGND, C1P and C1M must be < 3ohm

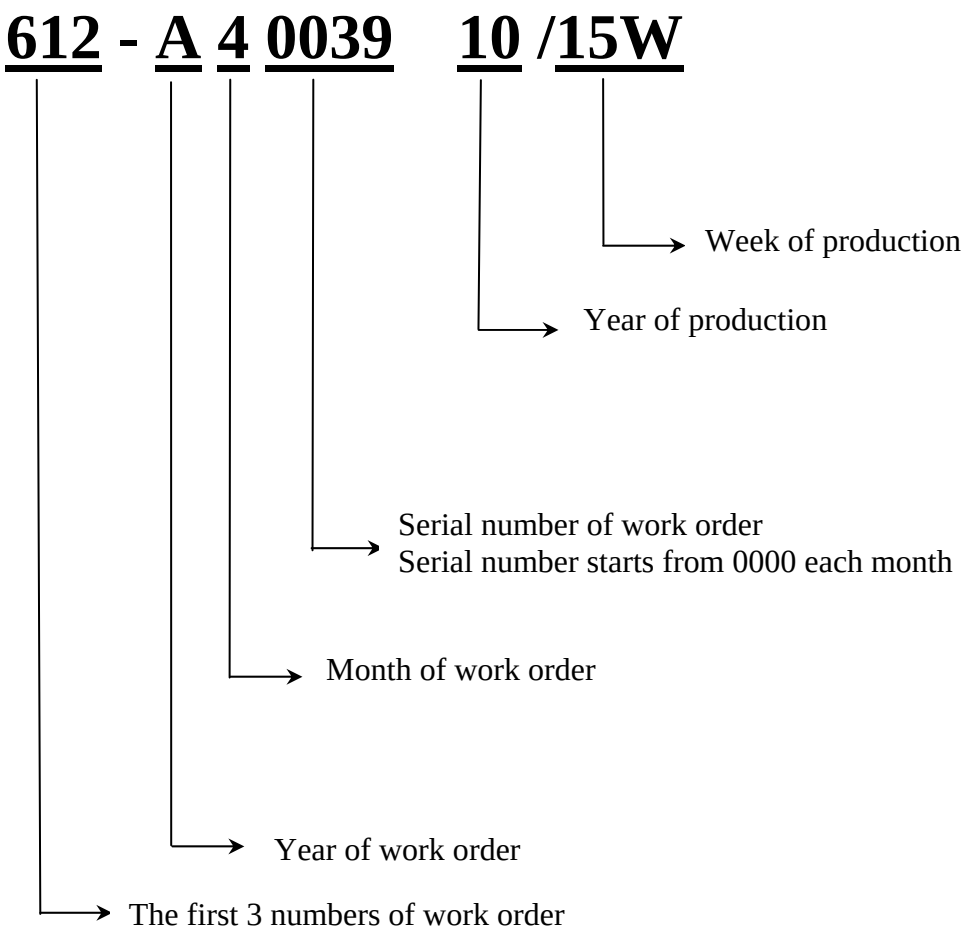
(4) B1 TO B4 use BEAD OR 0ohm

12.LCM PRODUCT LABEL DEFINE

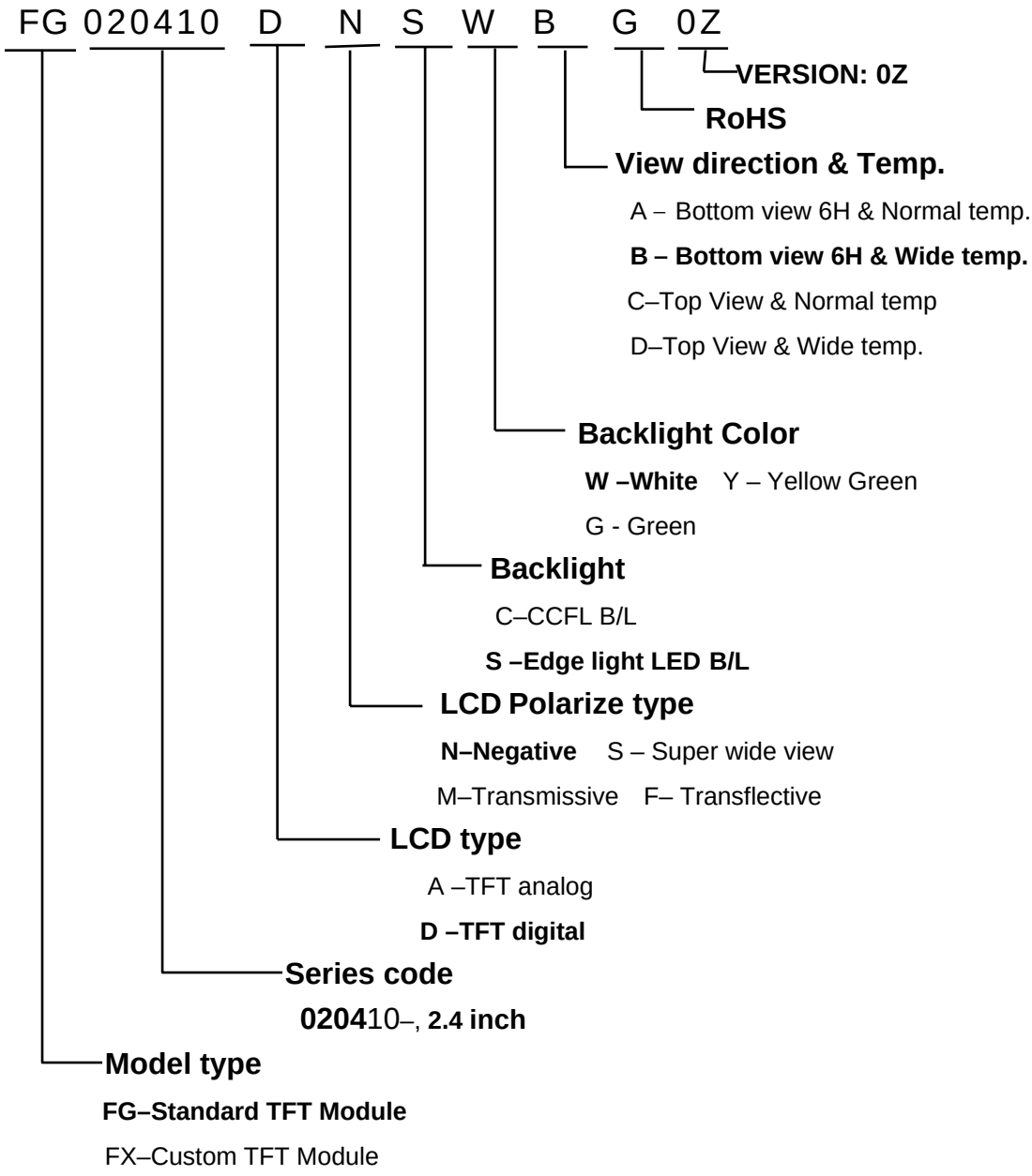
Product Label style:



Work order Define:



Product Name Define:



13.PRECAUTIONS IN USE LCM

1. LIQUID CRYSTAL DISPLAY (LCD)

LCD is made up of glass, organic sealant, organic fluid, and polymer based polarizers. The following precautions should be taken when handing,

(1). Keep the temperature within range of use and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel off or bubble.

(2). Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin.

(3). Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.

(4). Glass can be easily chipped or cracked from rough handling, especially at corners and edges.

(5). Do not drive LCD with DC voltage.

2. Liquid Crystal Display Modules

2.1 Mechanical Considerations

LCM are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.

(1). Do not tamper in any way with the tabs on the metal frame.

(2). Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.

(3). Do not touch the elastomer connector, especially insert an backlight panel (for example, EL).

(4). When mounting a LCM make sure that the PCB is not under any stress such as bending or twisting . Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.

(5). Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.

2.2. Static Electricity

LCM contains CMOS LSI's and the same precaution for such devices should apply, namely

(1). The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.

(2). The modules should be kept in antistatic bags or other containers resistant to static for storage.

(3). Only properly grounded soldering irons should be used.

(4). If an electric screwdriver is used, it should be well grounded and shielded from commutator sparks.

(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.

(6). Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

2.3 Soldering

(1). Solder only to the I/O terminals.

(2). Use only soldering irons with proper grounding and no leakage.

(3). Soldering temperature : 280°C ± 10°C

(4). Soldering time: 3 to 4 sec.

(5). Use eutectic solder with resin flux fill.

(6). If flux is used, the LCD surface should be covered to avoid flux spatters. Flux residue should be removed after wards.

2.4 Operation

(1). The viewing angle can be adjusted by varying the LCD driving voltage V0.

(2). Driving voltage should be kept within specified range; excess voltage shortens display life.

(3). Response time increases with decrease in temperature.

(4). Display may turn black or dark blue at temperatures above its operational range; this is (however not pressing on the viewing area) may cause the segments to appear "fractured".

(5). Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured".

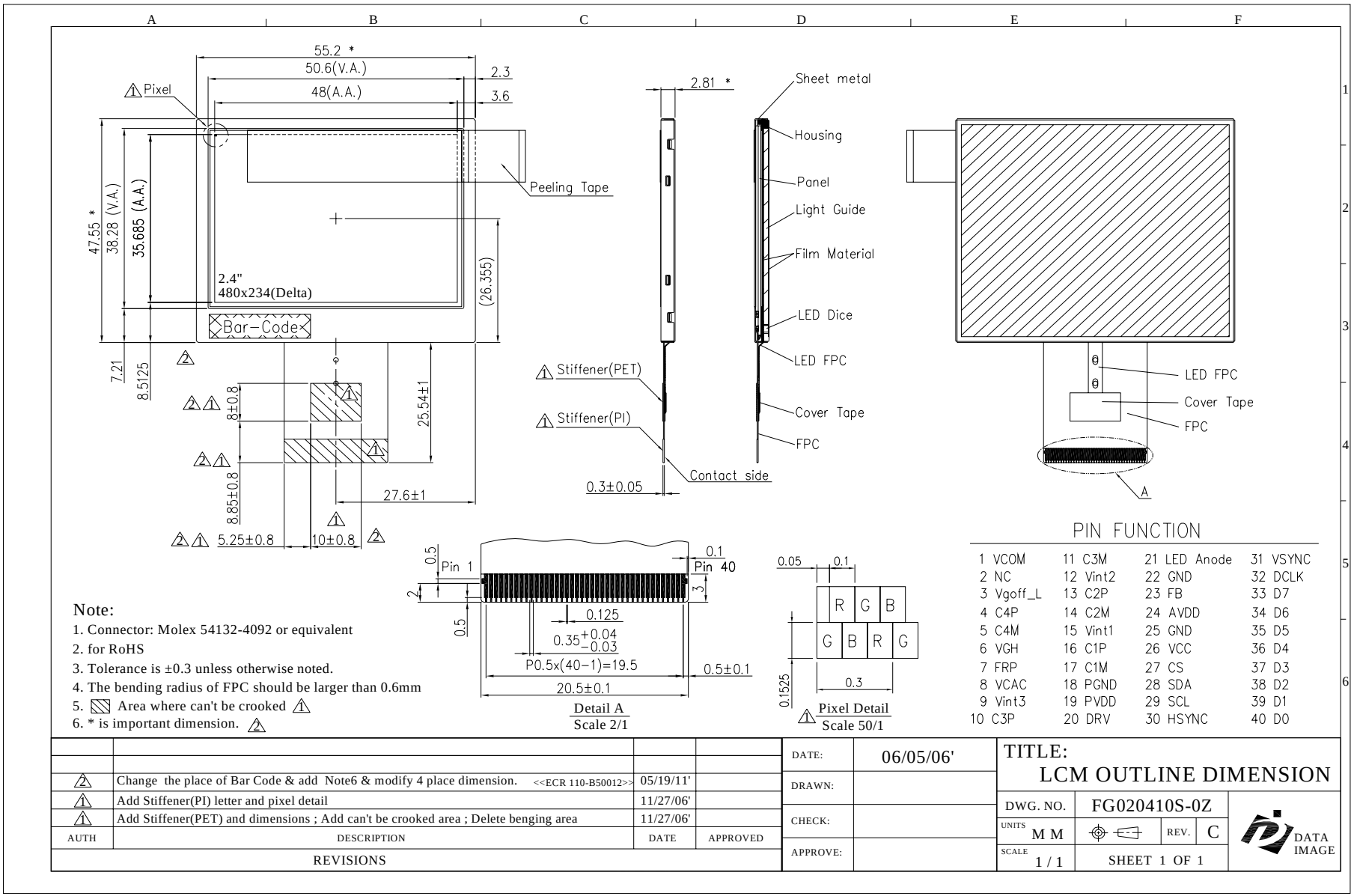
2.5 Storage

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all the time.

2.6 Limited Warranty

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.

14. OUTLINE DRAWING



Note:
1. Connector: Molex 54132-4092 or equivalent
2. for RoHS
3. Tolerance is ±0.3 unless otherwise noted.
4. The bending radius of FPC should be larger than 0.6mm
5. ▨ Area where can't be crooked ①
6. * is important dimension. ②

PIN FUNCTION

1 VCOM	11 C3M	21 LED Anode	31 VSYNC
2 NC	12 Vint2	22 GND	32 DCLK
3 Vgoff_L	13 C2P	23 FB	33 D7
4 C4P	14 C2M	24 AVDD	34 D6
5 C4M	15 Vint1	25 GND	35 D5
6 VGH	16 C1P	26 VCC	36 D4
7 FRP	17 C1M	27 CS	37 D3
8 VCAC	18 PGND	28 SDA	38 D2
9 Vint3	19 PVDD	29 SCL	39 D1
10 C3P	20 DRV	30 HSYNC	40 D0

AUTH	DESCRIPTION	DATE	APPROVED
②	Change the place of Bar Code & add Note6 & modify 4 place dimension. <<ECR 110-B50012>>	05/19/11'	
①	Add Stiffener(PI) letter and pixel detail	11/27/06'	
①	Add Stiffener(PET) and dimensions ; Add can't be crooked area ; Delete benging area	11/27/06'	

REVISIONS

DATE:	06/05/06'
DRAWN:	
CHECK:	
APPROVE:	

TITLE: LCM OUTLINE DIMENSION

DWG. NO.	FG020410S-0Z		
UNITS M M		REV.	C
SCALE 1 / 1	SHEET 1 OF 1		

DATA IMAGE

15.PACKAGE INFORMATION

Material

1 Carton + 2 Anti-static bag + 2 Form(35mm) + 20Anti-static tray + 2 Drier + 2 Antirust

Total pcs

1 Antistatic tray =10panel pcs

1 Anti-static bag = 9 Anti-static tray + cover tray =9*10 +1 = 90pcs

1 Carton = 2 Anti-static bag = 2*90 = 180pcs

1 Carton = 180 pcs

Carton size : 465L x 380W x 395H (mm)

Total Weight ≒5kgw

FG020410 TFT LCM PACKING