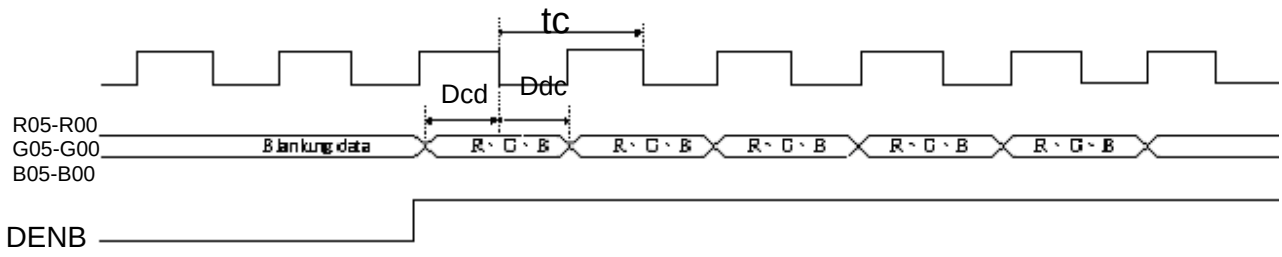
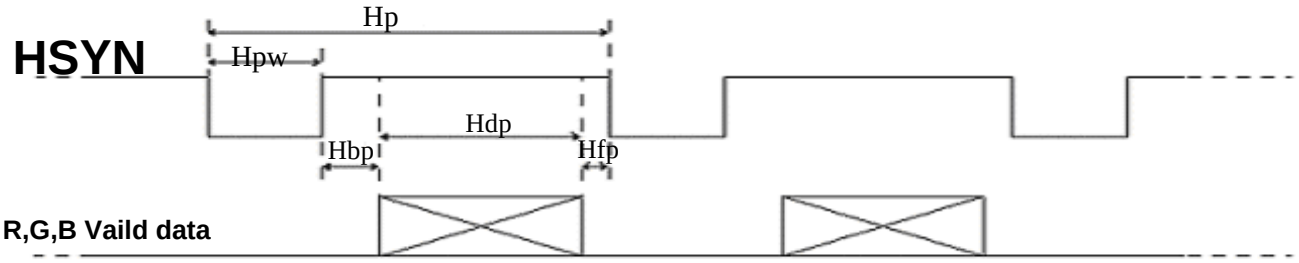
10-2) Timing Diagram

a.1 Input signal range



a.2 HSYNC timing



a.3 CLK,HSYNC relationship